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ORIGINAL

10^8 Bit Solid State Spacecraft Data Recorder

G. W. Murray, O. D. Bohning,
R. Y. Kinoshita, and F. J. Becker

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10^8 Bit Solid State Spacecraft Data Recorder

G. W. Murray, O. D. Bohning,
R. Y. Kinoshita, and F. J. Becker
Rockwell International
Anaheim, California

Prepared for
Langley Research Center
under Contract NAS1-14174

National Aeronautics
and Space Administration

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1.0 INTRODUCTION

This report describes the design, fabrication and test of a Solid State Spacecraft Data Recorder (SSDR) utilizing bubble domain memory technology. The SSDR represents a major milestone in the maturation of bubble domain technology from small scale laboratory demonstration systems to a large mass store flight configured system and marks another step in a series of NASA-Langley Research Center sponsored programs directed at the practical application of this technology. Specifically, this effort is based on and derived from memory element development done under NASA contract NAS1-12981 and system experience gained under NASA Contract NAS1-12435. The ultimate objective of these efforts is to develop a system which can provide a recording medium with no moving parts to replace tape recorders which have experienced unacceptably high failure rates in space applications. The specific purpose of the SSDR program is to provide a basis upon which a decision can be made relative to the applicability of bubble memory technology for this purpose.

While previous programs have dealt primarily with technology related directly to the memory element material, design, fabrication and operation, the SSDR program has addressed for the first time problems of organization, packaging and circuit design associated with large system application of bubbles. The data recorder system designed, built and tested on this program is a partially populated 10^8 bit memory which utilizes some of the unique characteristics of bubble domain memory technology to establish system capability and flexibility not possible with other mass storage mediums such as tape. The following sections describe the requirements established for the SSDR, design tradeoffs and configurations developed in response to these requirements and test results on hardware built to this design. Finally, an assessment is made of the results of this program in terms of achieving the goal of practical application of bubble memory to spaceborne applications and recommendations made for design changes in future systems.

Use of commercial products or names of manufacturers in this report does not constitute official endorsement of such products or manufacturers, either expressed or implied, by the National Aeronautics and Space Administration.

This report was prepared by Autonetics Strategic Systems Division, Electronics Systems Group, Electronics Operations of Rockwell International at Anaheim, CA under NASA Contract Number NAS1-14174. It summarizes work performed on this contract covering the period October 1, 1975 to March 1, 1978.

2.0 SSDR REQUIREMENTS

2.1 GENERAL

This section summarizes the initial requirements established for the Solid State Spacecraft Data Recorder in the Program Statement of Work. Design approaches developed in subsequent sections of this report are based on and evolved from these design goals.

The SSDR is intended to be a flight qualifiable model of a high reliability spacecraft data recorder using no moving parts and bubble domain technology as the primary storage medium. A general block diagram of the SSDR is given in Figure 2-1. Major elements of the SSDR are the Data Storage Subsystem (DSS), Drive and Control Unit (DCU) and Power Supply. The DSS contains the bubble memory and provides the capability of accessing and reading or writing into a designated memory address. Control of Data Flow between the user and the DSS is accomplished through the DCU. The power supply provides all secondary power required for SSDR operation. The following sections detail the design goals for each of these major subsystems.

2.2 DATA STORAGE SUBSYSTEM

The DSS is to be partitioned into memory modules which interface to redundant or multiple data and control buses. The memory modules in turn shall be partitioned into memory cells. The memory cells shall contain a minimum of eight memory elements with each element having a storage capacity of at least 1.024×10^5 bits. Each memory cell will have its own set of rotating field coils such that all memory elements within the cell operate in parallel. Any memory cell within the memory module may be addressed through the data and control bus. The memory module will include the electronics necessary to decode commands and addresses and control data flow between the memory cells and data buses. The DSS shall have a storage capacity equal to or greater than 1.024×10^8 bits.

2.3 DRIVE AND CONTROL UNIT

The DCU provides two primary functions in the SSDR. First, it serves to interpret commands by the SSDR user to generate the addresses and timing sequences required for the memory modules to perform the operation specified. In addition to this function, the DCU also provides configuration control to allow the SSDR to be operated either as a serial or parallel recorder and with a variable number of independent channels. The following sections detail these as well as additional design objectives for the DCU.

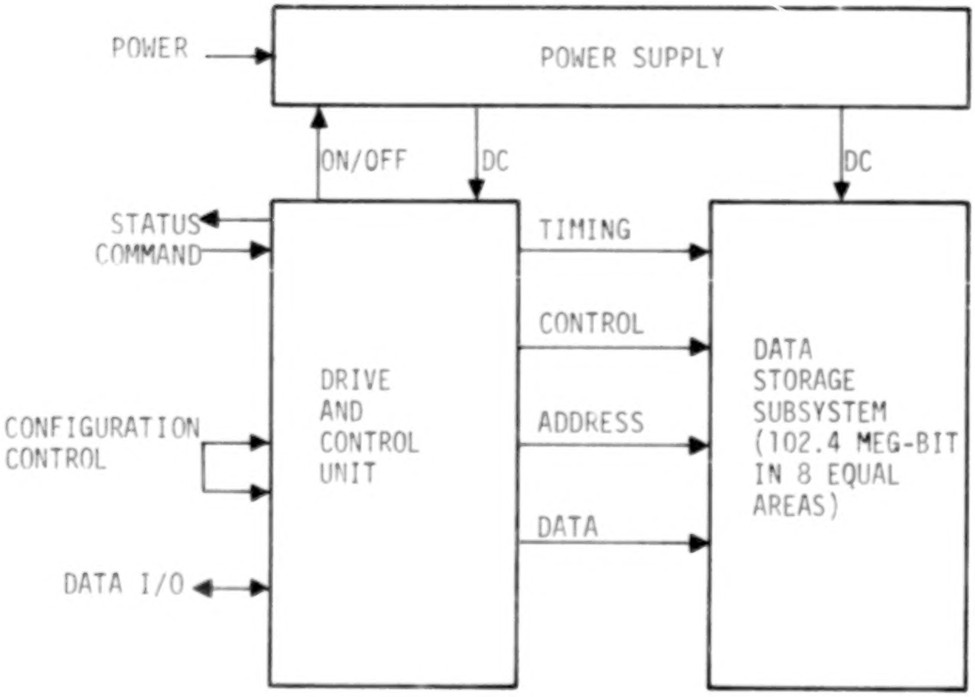
POWER
POWER SUPPLY
ON/OFF
DC
DC
STATUS
COMMAND
CONFIGURATION CONTROL
DATA I/O
DRIVE AND CONTROL UNIT
TIMING
CONTROL
ADDRESS
DATA
DATA STORAGE SUBSYSTEM (102.4 MEG-BIT IN 8 EQUAL AREAS)

Figure 2-1. SSDR Block Diagram

2.3.1 Data Interface and Configuration Control

Through the use of shorting jumpers on a configuration control connector, the recorder shall be capable of operating in a 1, 2, 4 or 8 channel serial mode with the DSS storage capacity allocated equally between the number of channels the SSDR is configured to provide. Data may be received or transmitted asynchronously on any channel up to a maximum of 1.2×10^6 bits/sec with the limitation that the composite data rate for all channels, both input and output, shall not exceed 2.4×10^6 bits/sec. A parallel input-output mode shall also be available which will allow the total DSS capacity to be accessed through a parallel data port which will accept 2, 4 or 8 bit byte. Data may be entered or read asynchronously in the parallel mode at rates up to 2.4 Mb/s.

2.3.2 Operating Modes and Commands

Operation of the SSDR shall be controlled by a set of sixteen commands which are provided by the user at a command and control connector. The command is implemented by a user generated execute signal which causes the SSDR to accept and perform the command present at the input to the command and control connector. The following defines the SSDR command set.

Solid State Spacecraft Recorder Command Set

RECORDER OFF - This command takes the recorder to a zero power state. Prior to powering down, the DCU shall store all housekeeping and status data in nonvolatile storage.

RECORDER ON - Applies power and places the SSDR in the standby mode.

INITIALIZE - Command places all channels in standby mode, clears all status flags, aligns all cells to the starting address and resets all address pointers to the starting address.

RESET (CHANNEL NUMBER) - Performs initialize operation on specified channel.

STANDBY - Internally generated status in which the SSDR awaits a command. In a multichannel configuration, it is possible for some channels to be in standby mode while others are not.

STOP (CHANNEL NUMBER) - Places specified channel in a standby mode after storing all status information such that the stopped operation may be resumed with a continue command.

CONTINUE (CHANNEL NUMBER) - Resumes an activity previously halted by a stop command or an interrupt.

ERASE (CHANNEL NUMBER) - For indicated channel, this command erases all data, sets address pointer to zero and places the channel in a standby mode.

WRITE (CHANNEL NUMBER) - Enables specified channel to receive data and write into the memory beginning at the zero address of the first cell allocated to that channel. A stop command is required at the end of a write sequence to empty the DCU data buffer into storage.

READ (CHANNEL NUMBER) - This command outputs stored data beginning at the zero address of the first cell assigned to the indicated channel and continues until the end of allocated storage is reached or a stop command is given.

GO TO X WRITE (CHANNEL NUMBER) - This command operates as an interrupt putting the present operation of the selected channel in a stop mode. The DCU then sets the channel address pointer to the start of the cell specified by X and writes new data while erasing old until the cell is full or a continue is received. If the cell is written full, the DCU will automatically generate a continue to resume the interrupted operation.

GO TO X READ (CELL NUMBER) - This command operates as an interrupt - putting the present operation of the selected channel in a stop mode. The DCU then sets the channel address pointer to the start of the cell indicated by X and reads the data until a continue command is given or the end of the cell is reached. If the total cell is read, the DCU will automatically generate a continue to resume the interrupted operation.

SKIP CELL (CHANNEL NUMBER, CELL NUMBER) - This command instructs the DCU to remove the designated cellfrom the allocated memory of the indicated channel. All other channels are unaffected.

SKIP CELL RESET (CHANNEL NUMBER, CELL NUMBER) - Removes a previously set skip cell command.

SET (CHANNEL NUMBER, CELL POINTER ADDRESS) - Aligns the record of the designated channel to the specified cell address.

EMERGENCY SHUTDOWN - A discrete command which instructs the recorder to shut down in an orderly manner in the event of an unscheduled power failure. The time between an emergency shutdown command and power loss shall be equal to or greater than one millisecond.

2.3.3 Status and Diagnostic Signals

A separate port will be provided on the SSDR to supply status and diagnostic information for telemetry and testing. Signals at this port will be of three types; system parameters, indicator flags and status.

2.3.3.1 System Parameters

Analog signals proportional to the parameters will be provided:

- DSS Temperature
- DSS Coil Drive Power
- DCU Power
- Total Power
- Secondary Voltages

2.3.3.2 Indicator Flags

Indicator flags are generated on a channel basis and are displayed continuously after the SSDR receives a parallel command code indicating the channel number requested. Indicator flags provided include:

- Standby
- Busy
- Beginning of Storage
- End of Storage
- Channel Full

2.3.3.3 Status

Status is generated on a channel basis and is displayed after receiving a parallel command code indicating the channel number requested. The status data includes the cell number of the last active cell and present mode of operation.

2.4 POWER SUPPLY

The SSDR power supply shall be designed as a modular unit which generates all required voltage for system operation from an input of 28 ± 4 volts D.C. Protection against input over-voltage or voltage reversal shall be provided. A goal for power consumption is defined as

$$P = 6 + 2 \times 10^{-5} f_T \text{ watts}$$

where f_T is the total composite data rate for the system.

2.5 MECHANICAL REQUIREMENTS

Goals for the mechanical design of the SSDR are established as follows:

Form Factor	- Rectangular parallelepiped with no side larger than four times the smallest side.
Volume	- 400 cubic inches
Weight	- 20 pounds.

The general mechanical design shall be such that the materials and construction of the SSDR shall meet the specified environmental requirements.

2.6 RELIABILITY

The design goal for SSDR system reliability using appropriate high reliability parts is a 20,000 hour MTBF with a 0.9 level of confidence. An error rate of equal to or less than 10^{-8} errors/bit is also a design objective.

2.7 ENVIRONMENTAL REQUIREMENTS

Design goals for the SSDR environment are as specified below.

Temperature

Operating	- -10 to 60°C
Data Retention	- -40 to 85°C
Survivability	- -50 to 125°C

Mechanical

Sine Wave Vibration	- Per MIL-STD-810B, Method 514. Levels per Part 1 of Procedure V, Curve Q.
Random Vibration	- Per MIL-STD-810B, Method 514 using Part 2 of Procedure V. Curve AK.
Acceleration	- ± 20 g's any axis for five minutes
Shock	- Per MIL-STD-810B, Method 516, Procedure I, Amplitude "A" and Duration "C".

Electromagnetic

Magnetic Field - Plus or minus 20 oe in any axis.

Conducted Susceptibility - Per MIL-STD-461/462, Methods CS01, CS02, and CS06.

3.0 SSDR ORGANIZATION

3.1 INTRODUCTION

In this section, the manner in which the detailed organization of the SSDR was evolved from the requirements of Section 2 is described. Considerations and tradeoffs involved in establishing the final design approach are reviewed and rationale given where the design deviates from requirements.

The starting point for this description of the organizational design of the SSDR are the two alternate SSDR configurations originally proposed in response to the Statement of Work. These two configurations are illustrated in Figures 3-1 and 3-2. Both versions consist of the same blocks, DCU, DSS, and Power. In both cases the Data Storage Subsystem and Power Supply Subsystem are basically identical. The total storage capacity of the DSS is divided into eight equal blocks with each block designated as a track. Each track consists of 13 Mb of storage along with circuitry required to read, write or align data within the track. Each of the tracks are totally independent allowing simultaneous operation of different modes in all eight tracks. This organization allows one track to be allocated to each channel in the eight channel mode of operation.

The difference between the two organizations is in the area of the Drive and Control Unit configuration. Both designs use a microprocessor as a master controller to interpret user commands and initiate the required operations within the DCU and DSS to carry out these commands. The organization of Figure 3-1 is configured on a channel basis with eight data buffers and controllers, one for each track of the DSS. A multiplexer network under microprocessor control directs data from the SSDR data port to the proper data buffer. Data transfer between data buffer and track is regulated by the channel controller which is also under microprocessor control. For eight channel operation, the multiplexer routes each of the eight data inputs directly to a data buffer. For four, two or one channel operation the multiplexer sequences through the two, four or eight data buffers respectively as each channel is read or written into. Such an organization is highly parallel and thus relatively free from disabling single points of failure but has the disadvantage of being rather complex.

The DCU configuration of Figure 3-2 is organized on a data bus basis. In this approach, there are two data buses, A and B, each of which go to all eight data buffers and eight tracks. Each data bus has a controller associated with it which can route the data between any of the eight buffers and any of the eight memory tracks. Data bus control is implemented through the controllers under the microprocessor master controller direction. For multichannel operation, the A and B data buses are time shared between the channels being used, with the microprocessor and bus controllers establishing which channel requires servicing and when. This design is considerably simpler than the channel controller configuration but can be susceptible to operational degradation due to single points of failure in the data bus/controller area.

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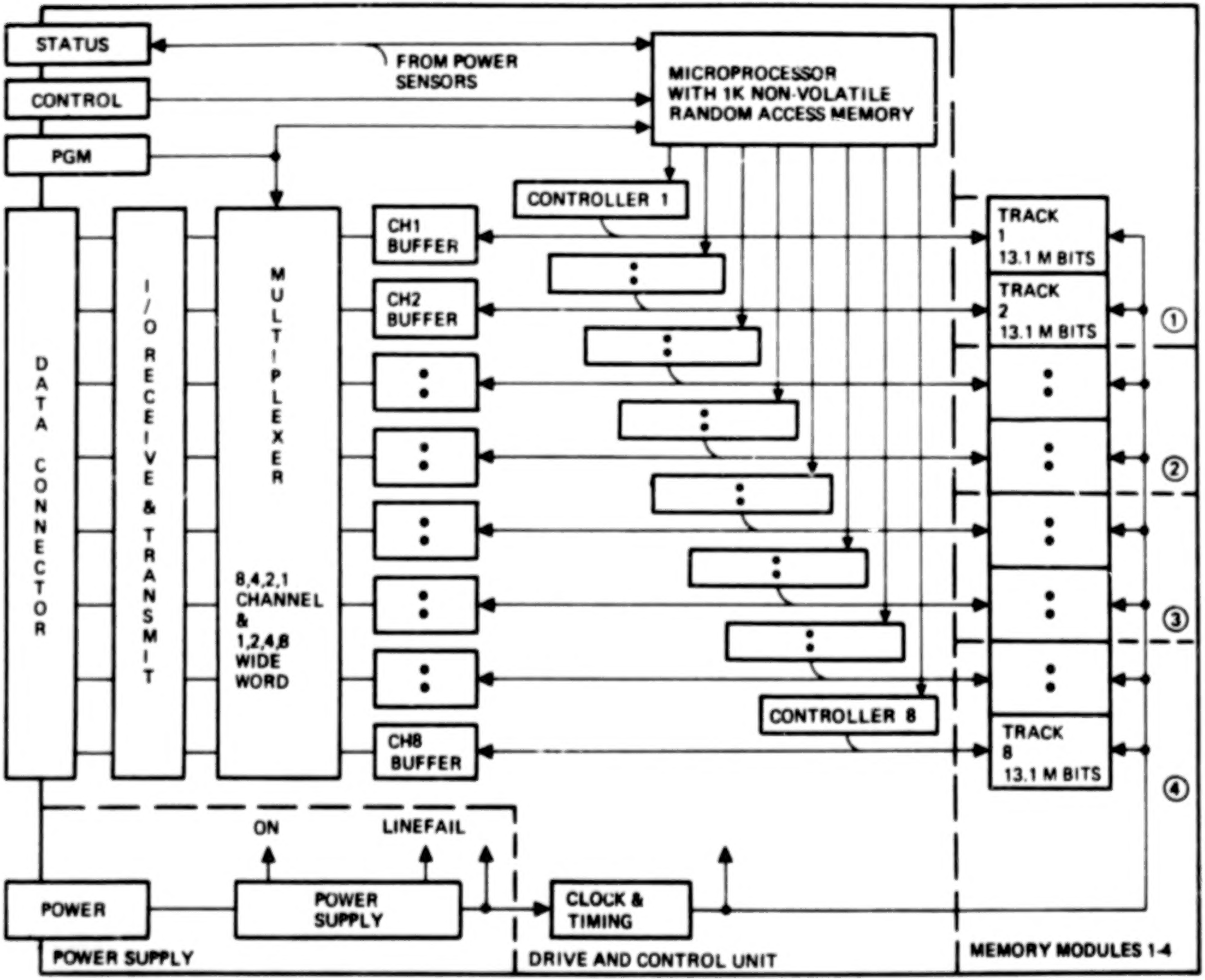

STATUS
CONTROL
PGM
FROM POWER SENSORS
MICROPROCESSOR WITH 1K NON-VOLATILE RANDOM ACCESS MEMORY
CONTROLLER 1
CONTROLLER 8
DATA CONNECTOR
I/O RECEIVE & TRANSMIT
MULTIPLEXER
8,4,2,1 CHANNEL & 1,2,4,8 WIDE WORD
CH1 BUFFER
CH2 BUFFER
CH8 BUFFER
TRACK 1 13.1 M BITS
TRACK 2 13.1 M BITS
TRACK 8 13.1 M BITS
①
②
③
④
ON
LINEFAIL
POWER
POWER SUPPLY
CLOCK & TIMING
POWER SUPPLY
DRIVE AND CONTROL UNIT
MEMORY MODULES 1-4

Figure 3-1. 10^8 Bit Recorder Using Individual Controllers

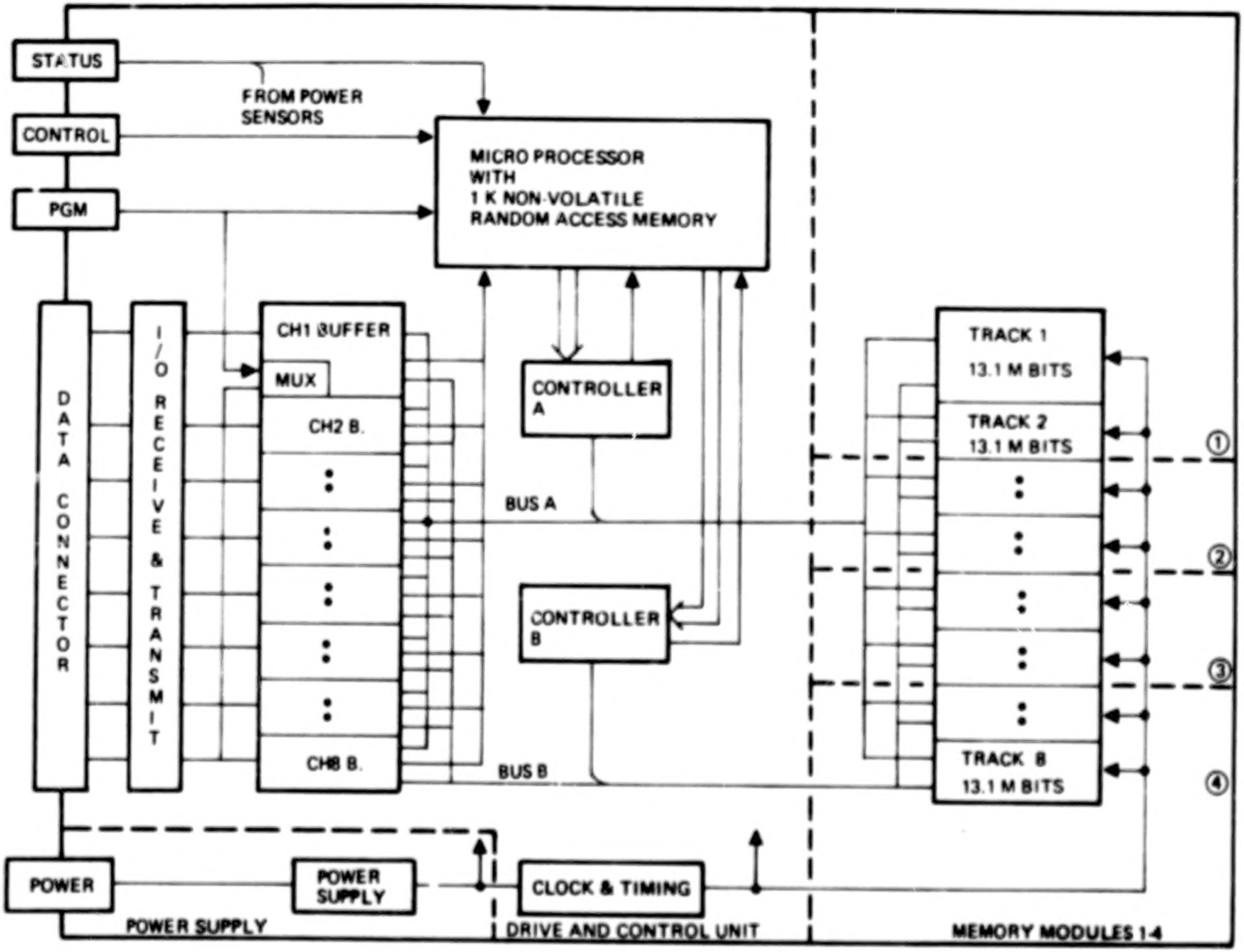

STATUS
FROM POWER SENSORS
CONTROL
PGM
MICRO PROCESSOR WITH 1 K NON-VOLATILE RANDOM ACCESS MEMORY
DATA CONNECTOR
I/O RECEIVE & TRANSMIT
CH1 BUFFER
MUX
CH2 B.
CH8 B.
CONTROLLER A
CONTROLLER B
BUS A
BUS B
TRACK 1 13.1 M BITS
TRACK 2 13.1 M BITS
TRACK 8 13.1 M BITS
①
②
③
④
POWER
POWER SUPPLY
CLOCK & TIMING
POWER SUPPLY
DRIVE AND CONTROL UNIT
MEMORY MODULES 1-4

Figure 3-2. 10^8 Bit Recorder Using Dual Controllers

The final SSDR organization has been derived from these first two initial designs. In the following two sections, the evolution of the Drive and Control Unit and Data Storage Subsystem organizations from this beginning are detailed.

3.2 DRIVE AND CONTROL UNIT ORGANIZATION

The first step in establishing a final DCU organization was to conduct a detailed analysis and tradeoff on the two originally proposed configurations. As described in the previous section, the primary difference between the two designs is the manner in which data multiplexing is accomplished within the DCU. In addition, the microprocessor control function was investigated in depth. Results and conclusions of this design analysis effort are summarized in the following two sections.

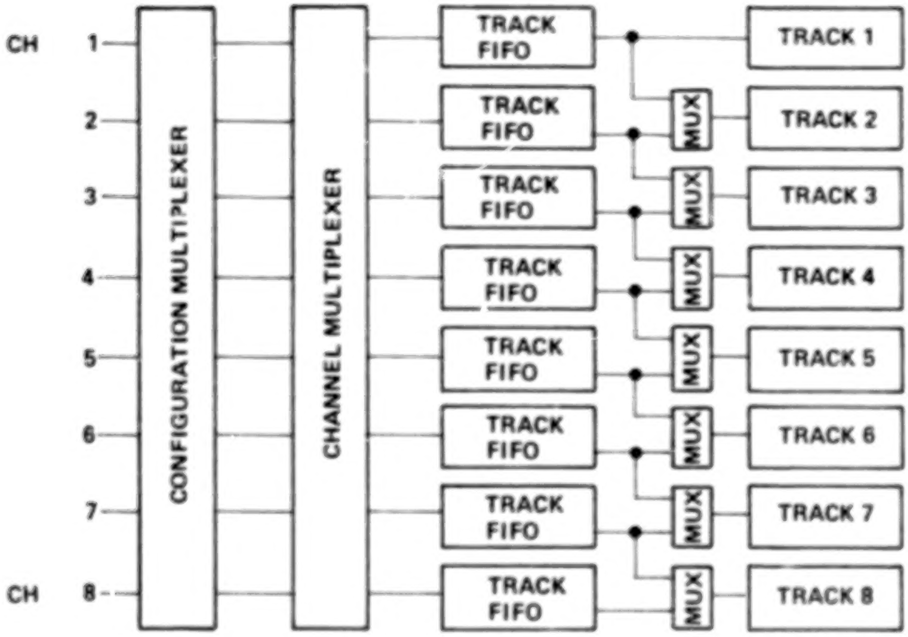
3.2.1 Data Multiplexing

The data path within the SSDR consists of up to eight independent bidirectional data channels at the recorder I/O interface, eight first-in-first out (FIFO) data buffers and eight bubble memory tracks. Interconnection of the blocks is both configuration and present address dependent. It is the manner in which this interconnection is made that is the subject of the data multiplexing investigation.

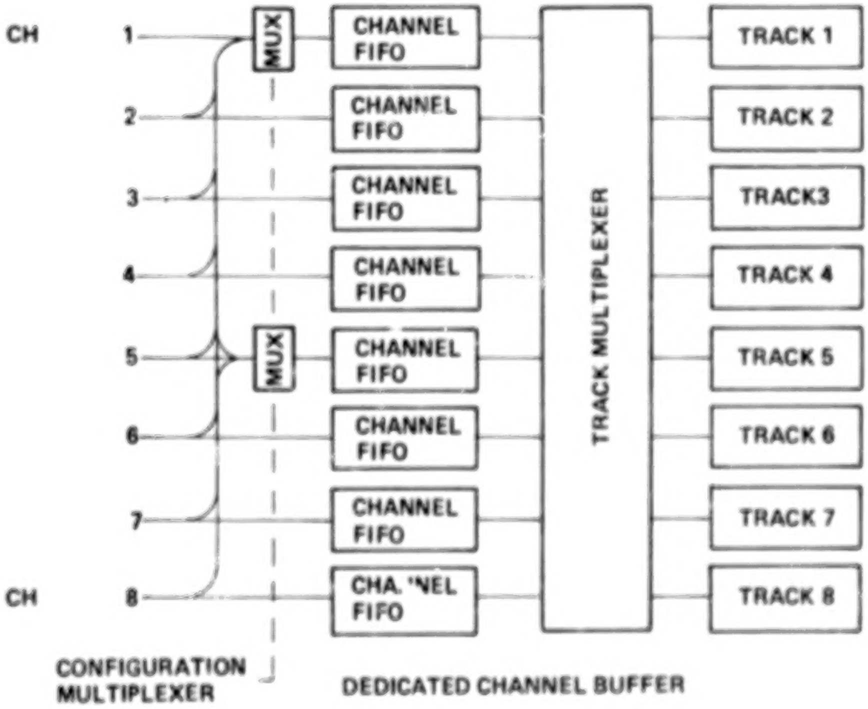
Two fundamental multiplexing techniques were evaluated. The first involves placing the bulk of the multiplexing hardware between the channel interface and the FIFO buffers, and thus dedicating the individual FIFO buffer to a single track. The alternate technique is to place the multiplexing hard-are between the FIFO buffers and the memory tracks and thus dedicating the buffers to the channel interfaces. The two techniques are diagrammed in Figure 3-3. The relative attributes of the two techniques are compared in Table 3-1.

A strawman mechanization of each technique was done using low power Schottky MSI TTL. Multiplexing for the dedicated track buffer technique, exclusive of control logic and FIFO buffers, required 90 IC's to mechanize. The mechanization uses multiple shift registers and multiple gated 2.5 MHz clock pulses and counters to hold the parts count down. This mechanization is diagrammed in Figures 3-4 and 3-5.

The ordered structure of the dedicated channel buffer leads directly to a multiple bus organization. Mechanization of the dual bus organization, again exclusive of control logic and FIFO buffers, required 66 IC's. This IC count is based on a parallel organization using one clock pulse per byte transfer. The single clock requires significantly simpler control logic than the multiple, gated clocks. The IC count includes redundant multiplexers to achieve full fault tolerance to a single channel failure while operating in a parallel bit configuration. The mechanization is diagrammed in Figure 3-6.


CH 1
2
3
4
5
6
7
CH 8
CONFIGURATION MULTIPLEXER
CHANNEL MULTIPLEXER
TRACK FIFO
MUX
TRACK 1
TRACK 2
TRACK 3
TRACK 4
TRACK 5
TRACK 6
TRACK 7
TRACK 8

DEDICATED TRACK BUFFER

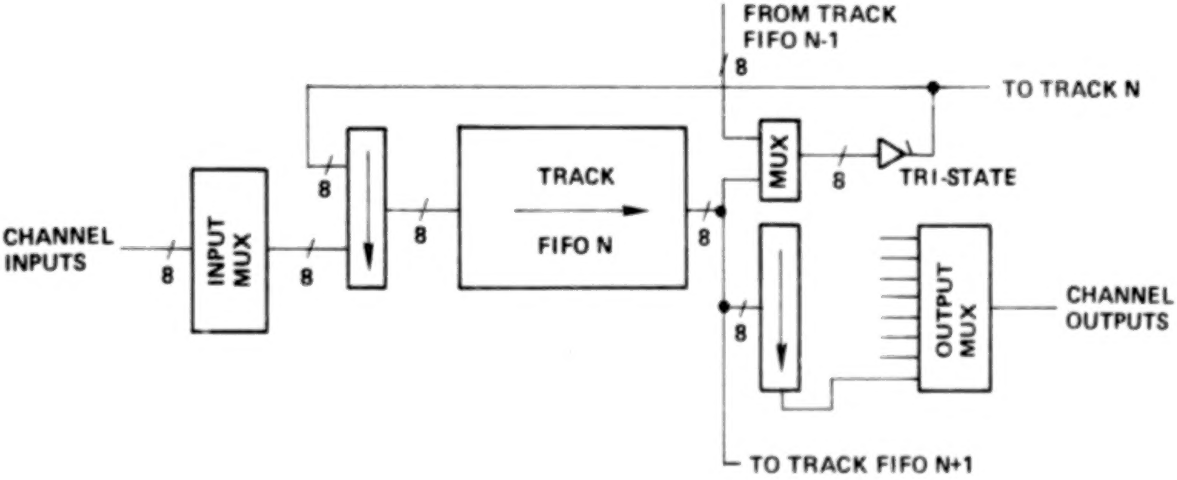

CH 1
2
3
4
5
6
7
CH 8
MUX
MUX
CHANNEL FIFO
TRACK MULTIPLEXER
TRACK 1
TRACK 2
TRACK3
TRACK 4
TRACK 5
TRACK 6
TRACK 7
TRACK 8
CONFIGURATION MULTIPLEXER

DEDICATED CHANNEL BUFFER

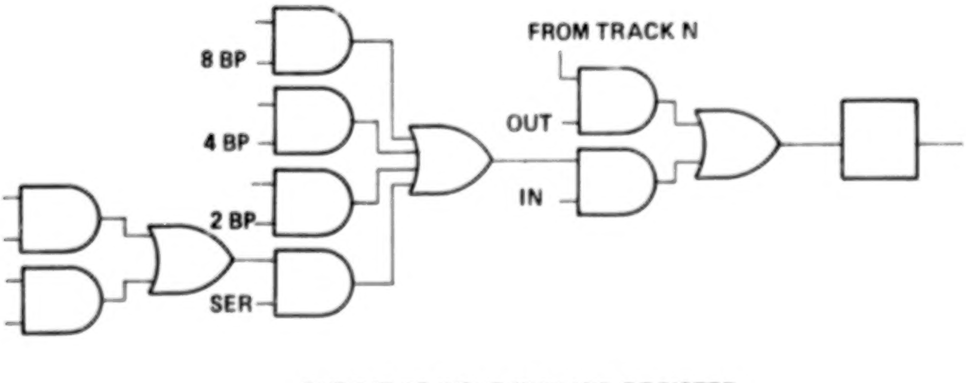
Figure 3-3. Data Multiplexing Techniques

Table 3-1. Attributes of Multiplexing Techniques

Dedicated Track Buffer	Dedicated Channel Buffer (Dual Data Bus)
Random structure	Ordered structure
More hardware and interconnects	Less hardware and interconnects
Function unique control	Universal control
Distributed, local timing and control	Centralized timing and control
Simplex transfers	Time multiplexed transfers
Transfers area limited	Transfers time limited
Static, multiple test points	Dynamic (snapshot) bus test points
Multiplexer faults impact access area, not time	Multiplexer faults impact access time, not area
Recorder configuration sensitive	Recorder configuration insensitive
Limited track expansion	Unlimited track expansion
Buffer fault implies loss of track (channel segment)	Buffer fault implies loss of channel


FROM TRACK
FIFO N-1
8
TO TRACK N
MUX
8
TRI-STATE
TRACK
FIFO N
CHANNEL
INPUTS
8
INPUT
MUX
8
8
8
8
8
OUTPUT
MUX
CHANNEL
OUTPUTS
TO TRACK FIFO N+1

ONE TYPICAL TRACK BUFFER


8 BP
4 BP
2 BP
SER
FROM TRACK N
OUT
IN

ONE BIT OF INPUT MUX AND REGISTER

Figure 3-4. Dedicated Track Implementation

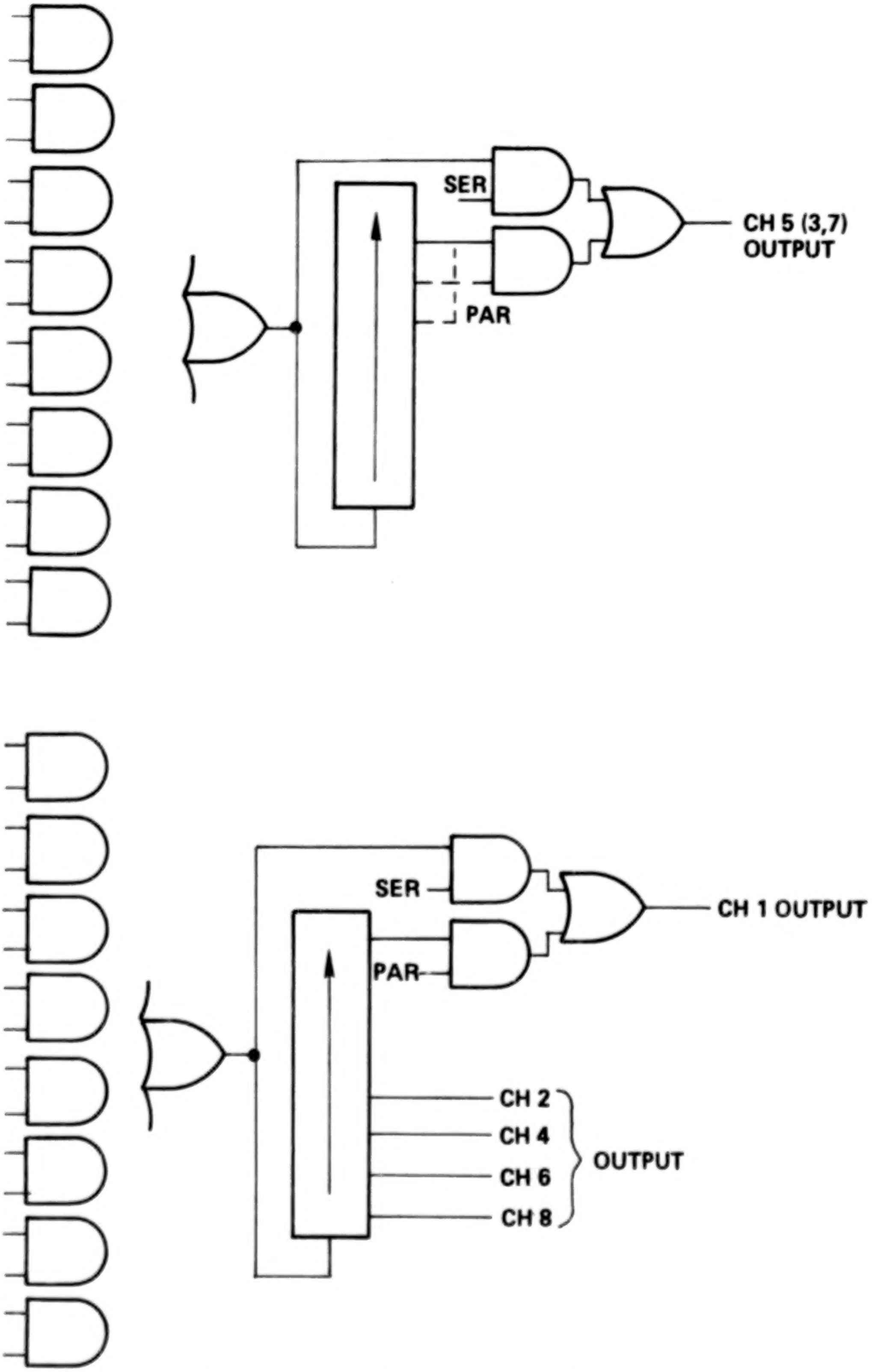
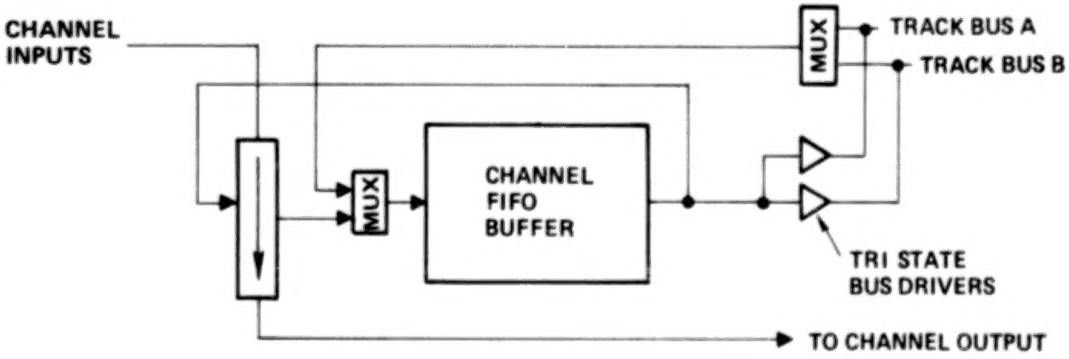
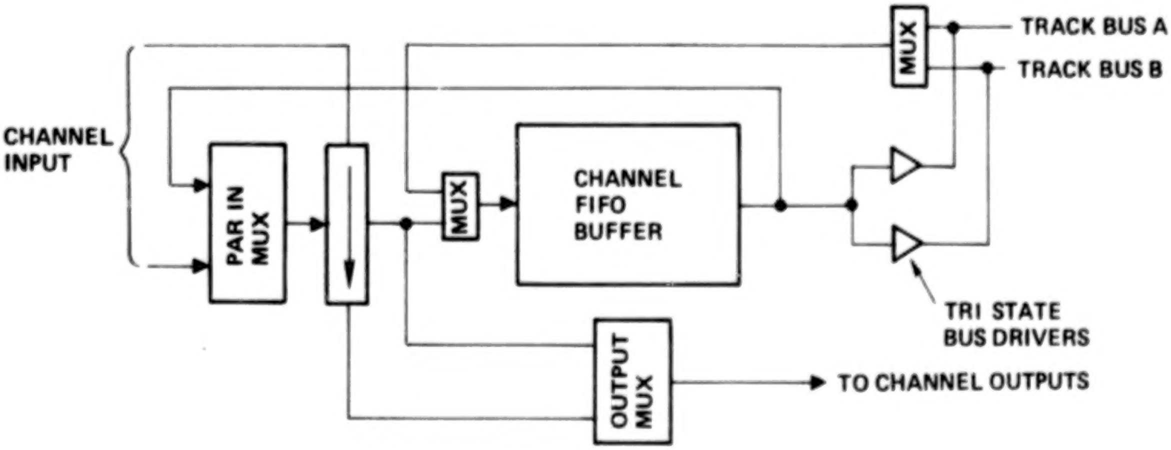

SER
CH 5 (3,7) OUTPUT
PAR
SER
CH 1 OUTPUT
PAR
CH 2
CH 4
CH 6
CH 8
OUTPUT

Figure 3-5. Dedicated Track Output MUX


CHANNEL
INPUTS
MUX
TRACK BUS A
TRACK BUS B
MUX
CHANNEL
FIFO
BUFFER
TRI STATE
BUS DRIVERS
TO CHANNEL OUTPUT

SERIAL CHANNEL


CHANNEL
INPUT
MUX
TRACK BUS A
TRACK BUS B
PAR IN
MUX
MUX
CHANNEL
FIFO
BUFFER
TRI STATE
BUS DRIVERS
OUTPUT
MUX
TO CHANNEL OUTPUTS

PARALLEL CHANNEL MUX

Figure 3-6. Dedicated Channel Implementation

Based on this evaluation, the dual data bus organization would appear to be preferable over the dedicated track organization.

3.2.2 Microprocessor Control

In the originally proposed DCU configuration, hardware controllers were used for the bulk of the real time control of the recorder. A microprocessor was used in the background to act as a scheduler and supervisor to interpret user commands, initiate operations, and to provide status information to the user. Detailed analysis indicates that it is desirable to integrate the microprocessor into the real time functions of the recorder. Such an approach more efficiently utilizes the flexibility of the microprocessor and reduces total system hardware requirements. When considered in terms of the dedicated channel buffer/multiple bus organization, two possible organizations emerge as being the most reasonable.

The first organization, referred to as the "smart channel" organization, has a microprocessor dedicated to each of the eight independent recorder channels. A block diagram of this organization is in Figure 3-7. The second, the "smart bus" organization uses a microprocessor in each of the two bus controllers as shown in block diagram in Figure 3-8. The attributes of the two organizations are compared in Table 3-2.

In the "smart channel" organization, the eight independent channel microprocessors make requests to the dual bus controllers as necessary. The first available bus controller responds, giving the requesting channel access to the bus until the request is satisfied. All channel status information is resident with the channel controller. User channel commands are vectored to the desired channel. Recorder commands (Recorder Off, Initialize, etc.) are handled by the channel preassigned to the task by the user. Preassignment is made by setting a nonvolatile Master Pointer register of 3 bits or less.

In the "smart bus" organization, the channel requests are serviced by the first available bus controller. The smart bus controller obtains the status of the requesting channel from the center status pool, a fast read/write memory. The status pool is updated at the conclusion of the request. All user commands are handled by the master bus controller. The master bus controller is preassigned by the user by setting the 1 bit non-volatile Master Pointer.

In a comparison between the two hardware approaches, both using a dual bus approach, there are several software considerations to take into account. These can be divided up into two major categories: (1) system considerations and (2) track controller considerations.

In the "smart bus" approach, the two CPU's must decide which one of them will respond to a command from the user computer. Then there must be a decision as to which CPU will execute the command and when. For example, if CPU A is currently executing a command for channel 2 and CPU B responds to the next command, which also pertains to channel 2, CPU A must be the one to execute the new command even though CPU B is idle.

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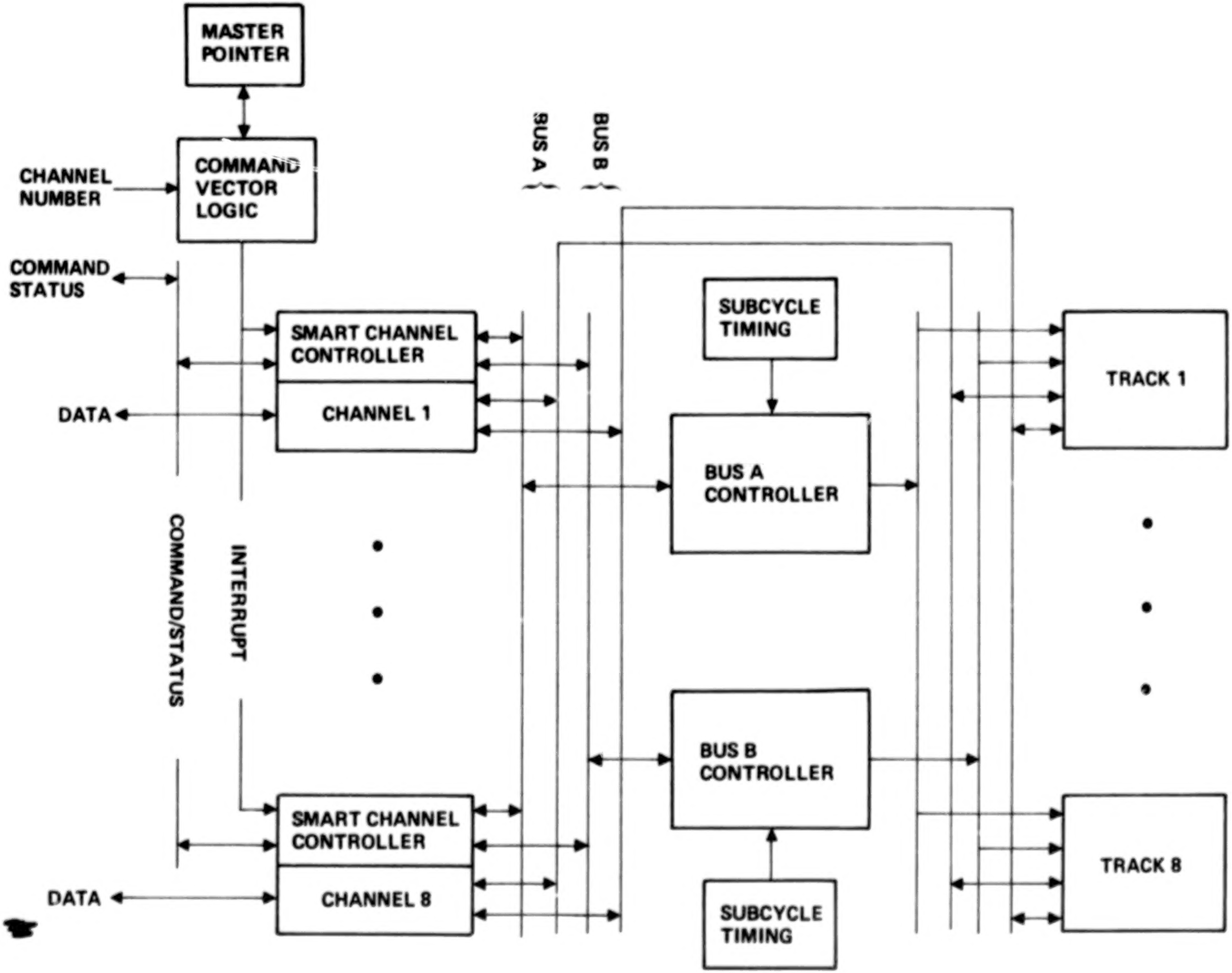
MASTER POINTER
CHANNEL NUMBER
COMMAND VECTOR LOGIC
COMMAND STATUS
BUS A
BUS B
SMART CHANNEL CONTROLLER
CHANNEL 1
DATA
SUBCYCLE TIMING
TRACK 1
BUS A CONTROLLER
COMMAND/STATUS
INTERRUPT
BUS B CONTROLLER
SMART CHANNEL CONTROLLER
CHANNEL 8
DATA
TRACK 8
SUBCYCLE TIMING

Figure 3-7. Smart Channel DCU Organization

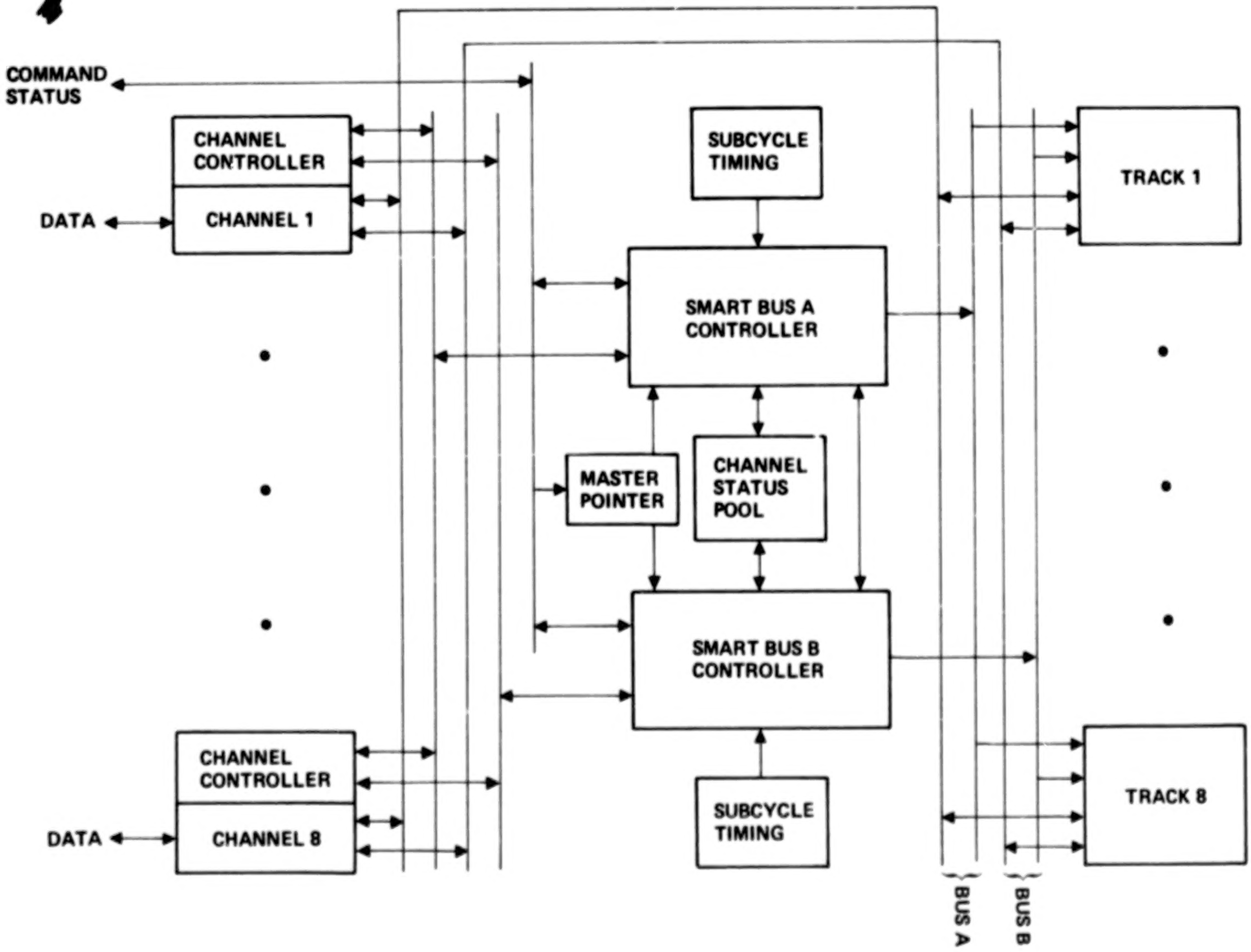
COMMAND
STATUS
CHANNEL CONTROLLER
CHANNEL 1
DATA
SUBCYCLE TIMING
TRACK 1
SMART BUS A CONTROLLER
MASTER POINTER
CHANNEL STATUS POOL
SMART BUS B CONTROLLER
CHANNEL CONTROLLER
CHANNEL 8
DATA
SUBCYCLE TIMING
TRACK 8
BUS A
BUS B

Figure 3-8. Smart Bus DCU Organization

Table 3-2. Multiprocessor Organization Attributes

Smart Channel	Smart Bus
Independent tasks	Status interdependent tasks
Single program tasks	Multi program tasks
Duplicate hardware	Consolidated hardware
Status stored locally	Status remotely pooled
8 minimal performance microprocessors required	2 high performance microprocessors required
Microprocessor fault implies loss of channel	Microprocessor fault implies reduction in performance

Commands that are not completed, yet are not being executed, must be completed by a CPU that is idle. Reassigning unfinished commands to the two CPU's must also be considered. Commands pertaining to channels whose prior command had not been completed must also be watched for.

In the "smart channel" approach, system considerations are somewhat less complex. First, each CPU must be smart enough to respond to a command for it. Then, there must be some way for the eight channel controllers to multiplex use of the two buses so that no data is lost from the buffers. It must be decided when a channel can control a bus, which channel can control, and which bus it can control.

Track controller considerations are more or less identical for the two different approaches. Each CPU that controls the bus must power down the track if the FIFO is empty/full for a write/read, it is at EOC (End of Cell), or the MEA (Memory Element Address) equals the WRTPTR (Write Pointer). The CPU must change cells at EOC, update the MEA and WRTPTR, do proper bookkeeping and switch operations on an interrupt, and make sure the hardware comparator is gated correctly. In the "smart channel" approach, the CPU must relinquish control of the bus whenever the FIFO is empty or full or upon completion of a command. In the "smart bus" approach, the CPU must be capable of switching to a different channel which is more critically in need of the bus.

In conclusion, it would be considerably simpler to program the "smart channel" implementation of the "smart bus" approach.

Based on the considerations discussed above, a "smart channel" multiprocessor organization was selected as being the best compromise to efficient DCU control.

3.2.3 Final DCU Organization

A more detailed design of the DCU was undertaken using a dedicated channel, multiple bus organization with a "smart channel" control implementation. As detailed parts list and power estimates were made for this design, it became apparent that there were problems in meeting system design goals with this design. The estimate of the original design DCU included a microprocessor and about 400 IC's with a typical power dissipation of 16 watts in the eight channel mode. The new modified design used eight microprocessors and 300 IC's with a typical power dissipation of 44 watts in an eight channel mode. This power level is clearly undesirable.

The increase in power in the design could be attributed almost totally to the increase in the number of microprocessors from one to eight. However, this additional use of microprocessors did result in an estimated 25% reduction in DCU parts and would have a direct and significant impact on system weight and volume. Thus the tradeoff reduces to one of weight and volume versus power. However, this trade must be weighed further by the judgement that the modified design is a more practical and lower risk approach to the DCU configuration. After considering the various options available and discussing the alternative with NASA-Langley Research Center it was decided that the best compromise would be to use the proposed new design but to reduce the number of possible channels to a maximum of four.

This reduces the number of microprocessors required from eight to four, reduces maximum DCU power by 19 watts and gives a 200 part reduction in IC count with a corresponding increase in board area of about 150 in^2. At this time it was also decided to constrain the parallel mode to an eight bit wide interface and remove the options for two and four bit wide interfaces. This change eliminated 22 IC's and reduced maximum power by 1.6 watts.

3.3 DATA STORAGE SUBSYSTEM ORGANIZATION

The original approach proposed for the Data Storage Subsystem divided the SSDR storage capacity into eight independent memory tracks. A general block diagram of the initial DSS design is illustrated in Figure 3-9. The track consisted of sixteen memory cells of eight memory elements each for a total capacity of 13,107,200 bits per track. Operation of the track is controlled by the DCU through the timing and control interface of the track. An address term selects the track and the particular cell within the track to be accessed. The mode term at the track interface establishes the operation to be performed and applies power through the power control section to the circuitry required for the commanded operation. All other circuitry is unpowered to minimize power consumption. Under timing control provided by the DCU, coil drive is applied to the addressed cell allowing data to be read or written through the track data interface. Coil drive, operator and sense circuitry were intended to be multiplexed over the sixteen cells in the track to minimize parts.

As preliminary design was started on the DSS and the DCU configuration was being established, it became obvious that the original DSS configuration should be modified. The first change in the DSS was made strictly in response to the reduction in number of SSDR channels from eight to four. This change implied that the number of tracks could be reduced to four. Under these conditions, the track organization would remain as in Figure 3-9, but the number of cells increased from sixteen to thirty-two. In this same time frame preliminary cell design had resulted in a decision to increase the number of chips/cell from eight to sixteen (details of the memory cell design is discussed in Section 4.0). Thus the DSS was composed of four tracks identical to that of Figure 3-9 but with sixteen chips per cell.

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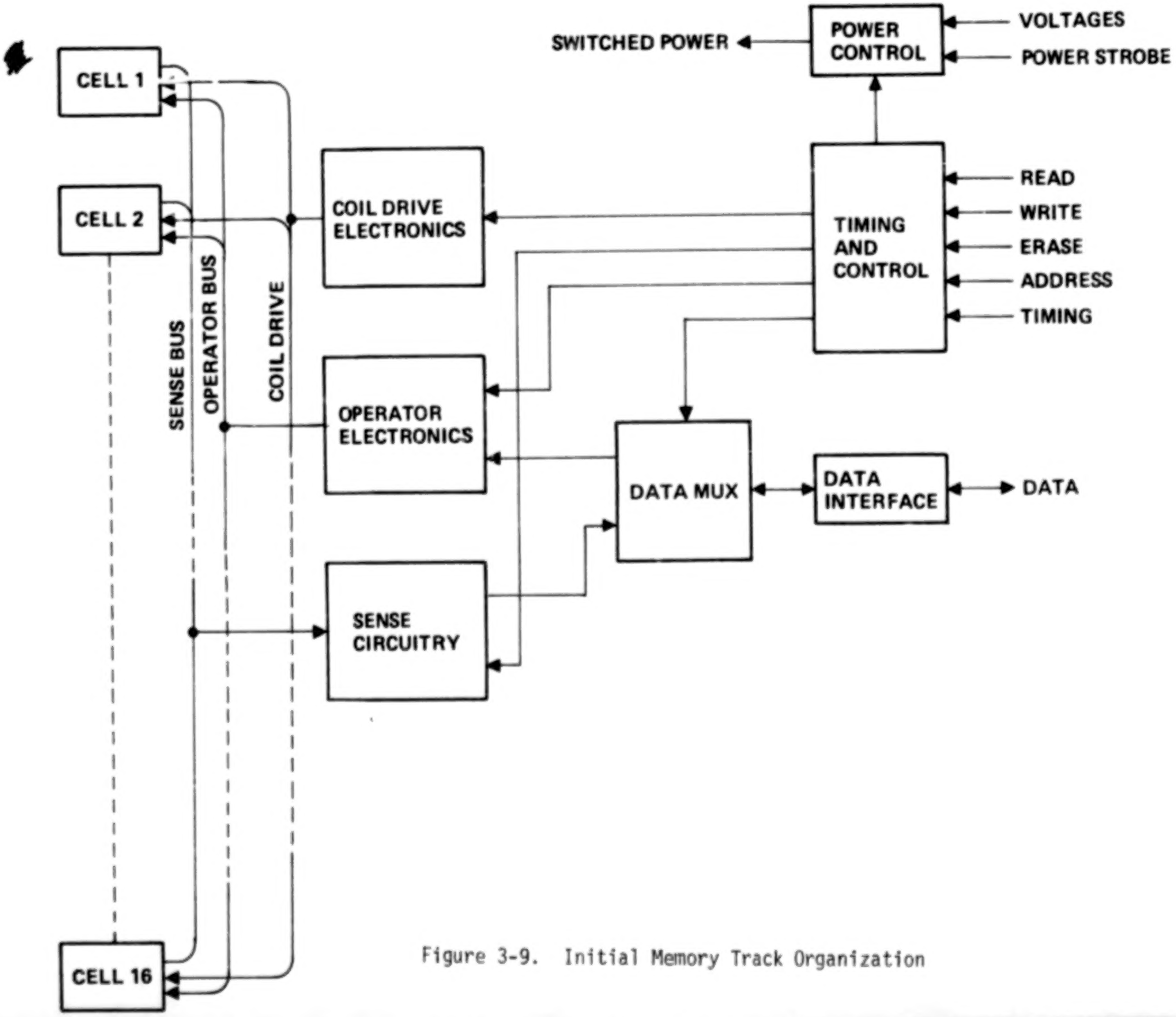
TRACK INTERFACE
SWITCHED POWER
POWER CONTROL
VOLTAGES
POWER STROBE
CELL 1
CELL 2
CELL 16
COIL DRIVE ELECTRONICS
TIMING AND CONTROL
READ
WRITE
ERASE
ADDRESS
TIMING
SENSE BUS
OPERATOR BUS
COIL DRIVE
OPERATOR ELECTRONICS
DATA MUX
DATA INTERFACE
DATA
SENSE CIRCUITRY

Figure 3-9. Initial Memory Track Organization

Using this configuration, preliminary parts list and mechanical designs were generated allowing an estimate of total SSDR weight, volume and power to be made. The results of this analysis compared to Statement of Work goals is summarized below.

Source	Weight	Volume	Power
S.O.W.	20	400 in^3	54 watts max.
Review Design	63	914 in^3	110 watts max.

As is obvious from this summary, there was a serious and most probably unacceptable problem with these characteristics. Because of this, it was extremely important to develop means by which these parameters could be brought more in line with program goals. There appeared to be two basic approaches to achieving this objective. The first involved developing more efficient designs of the proposed system to generate a smaller and lighter package while the second approach considered modification of system capability requirements to achieve a simpler and, therefore, more mechanically efficient package. The following sections discuss the approaches and tradeoffs for both of these techniques.

The first step in developing a more efficient design of the proposed system was to determine which areas contributed most heavily to the problem and would thus benefit most from improvement. A breakdown for the four track design is given in Table 3-3. The first and most obvious conclusion of this data is that any significant reductions must come from modifications in the DSS which makes up 76% of the SSDR weight and 77% of the SSDR volume.

From an organizational standpoint it would be possible to reduce volume and weight by modifying some functional design objectives to allow the use of more efficient DSS organizations. Primary in this regard is a reduction of the number of tracks on the DSS. The use of four tracks in the design was selected for two primary reasons. The first reason was in order to obtain the required 2.4 MHz total data rate it must be possible to access two tracks simultaneously; this implies a set of operator/sense and coil drive electronics for each channel. The second reason is that this organization tends to minimize the impact of DSS electronics failures in terms of the amount of memory lost by a single failure. However, these advantages are gained at the expense of a large parts count and volume associated with this organization.

If the DSS organization is reduced to one or two tracks, savings in weight, volume and parts count may be realized. In such an organization, a four channel mode is still possible but the allocation of memory to channel is basically a part of the DCU software with the memory capacity of a track divided between two or four channels for a two and one track organization respectively. The penalty which must be paid for these organizations in terms of susceptibility to single point failures is obvious; however, the impact on total SSDR data rate is not as severe as might be expected. The data rate problem occurs when parallel access of two channels contained on a single track

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Table 3-3. SSDR Estimated Weight-Volume-Parts Summary

Item	Weight-Lb					Volume-In^3		Parts Count		
	Ea	Per MM	Per DSS	Per SSDR	% SSDR	% SSDR	Per SSDR	Ea	Per SSDR	% SSDR
1. Dual Cell-Bias Assy	0.555	4.440	17.760	17.760	28.2	11.7	107			
1.1 Cel (pr)	0.232	1.856	7.424	7.424	11.8	5.0	46			
1.2 Bias Assy	0.323	2.584	10.336	10.336	16.4	6.7	61			
1.2.1 Bias NI-FE	0.185	1.480	5.920	5.920	9.4	-	-			
2. Memory Module (MM)	12	12	48	48	76.2	77.0	704	1486	5944	92.8
2.1 Dual Cell-Bias Assy	0.555	4.440	17.760	17.760	28.2	11.7	107			
2.2 Frame	1.156	1.156	4.624	4.624	7.3	-	-			
2.3 MLB-Comps-Rails	5.296	5.296	21.184	21.184	33.6	57.3	524			
2.3.1 Sense-Operator (40%)	2.118	2.118	8.472	8.472	13.4	17.1	156	505	2020	31.5
2.3.2 Coil Drivers (60%)	3.178	3.178	12.712	12.172	20.2	40.2	368	981	3924	61.3
2.4 Misc	1.108	1.108	4.432	4.432	7.1	-	-			
3. DCU-Base Plate	5	-	-	5	7.9	10.1	93	463	463*	7.2
3.1 Frame	1.267	-	-	1.267	2.0	-	-			
3.2 MLB-Comps-Rails	3.310	-	-	3.310	5.2	7.8	71			
3.3 Misc	0.423	-	-	0.423	0.7	-	-			
4. I-O Box Assy	0.658	-	-	0.658	1.0	3.3	30			
5. Power Supply	5.5	-	-	5.5	8.7	8.1	74	(TBD)	(TBD)	(TBD)
6. SSDR	63	-	-	$\boxed{63}$	100	100	$\boxed{914}$	6407	$\boxed{6407}$	100
6.1 Memory Module	12	12	48	48	76.2	77	704	1486	5944	92.8
6.2 DCU-Base Plate	5	-	-	5	7.9	10.1	93	463	463*	7.2
6.3 I-O Box	0.658	-	-	0.658	1.0	3.3	30	-	-	-
6.4 Power Supply	5.5	-	-	5.5	8.7	8.1	74	(TBD)	(TBD)	(TBD)
6.5 Covers	1.924	-	-	1.924	3.1	1.5	13	-	-	-
6.6 Misc	1.918	-	-	1.918	3.1	-	-	-	-	-

*NOTE: +512 cores

is requested as single track electronics can only process one request at a time. However, the data rate internal to the MM is 2.4 MHz (16 chips at 150 KHz) allowing parallel access to two channels on the same track in a time multiplexed mode with a total data rate which would approach 2.4 MHz. The actual data rate achieved would depend on minimum data block length and DCU commutating time. It should be noted that parallel access into two tracks of the two track organization could still achieve the 2.4 MHz data rate.

There are two additional characteristics of a one or two track organization which should be mentioned. First it should be noted that although susceptibility to single point failures is increased, parts count is significantly reduced and as a result system MTBF can be expected to increase. Secondly, the impact of organization on cost is significant. The amount of labor and parts in a two or one track organization is significantly less than that of a four track system and this would be reflected in the production cost of the SSDR.

Based on the above discussions, three possible alternatives for DSS organization were suggested. Each of the three emphasize different aspects of the SSDR program goals. The particular approach selected is basically dependent on the priorities placed on various program objectives. These three organizations are described in the following section.

Model 1 - The organization of Model 1 SSDR is illustrated in Figure 3-10. This system is formulated to achieve a maximum number of SSDR functional goals at the expense of weight and volume. Basically this configuration is the same as described in this system design data package with the exception of using a matrixed trapezoid coil drive system with hybridized power transistors. This appears to be the most optimum approach to achieving SSDR functional goals in the minimum weight and volume at this state of bubble memory technology.

Model 2 - Model 2 represents an approach which seeks to achieve a balance between the functional and mechanical goals for the SSDR. This organization is illustrated in Figure 3-11. This organization is a two track version of the Model 1 system with each track containing 2 x the memory capacity of a Model 1 track. The reduced parts count and volume is achieved at the expense of slightly reduced data rate and increased potential impact of single failures on memory capability. It should be noted that the production cost of this model will probably be significantly less than that of Model 1.

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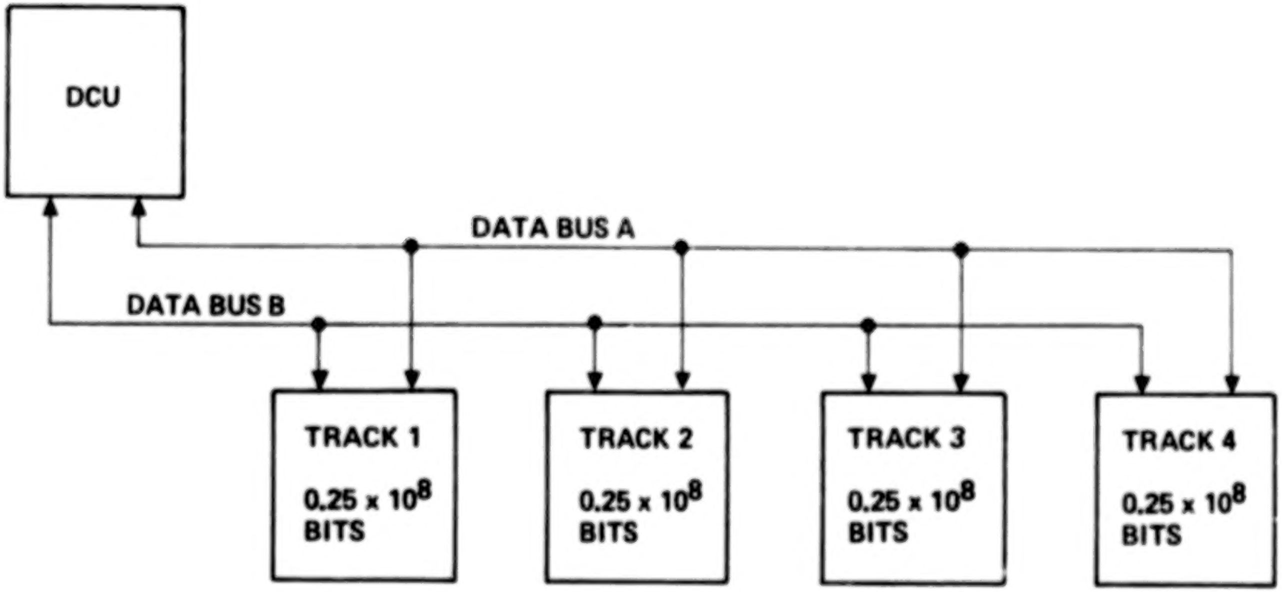

DCU
DATA BUS A
DATA BUS B
TRACK 1
0.25 x 10⁸ BITS
TRACK 2
0.25 x 10⁸ BITS
TRACK 3
0.25 x 10⁸ BITS
TRACK 4
0.25 x 10⁸ BITS

CHARACTERISTICS

CAPACITY – 10^8 BITS

VOLUME – 620 IN^3

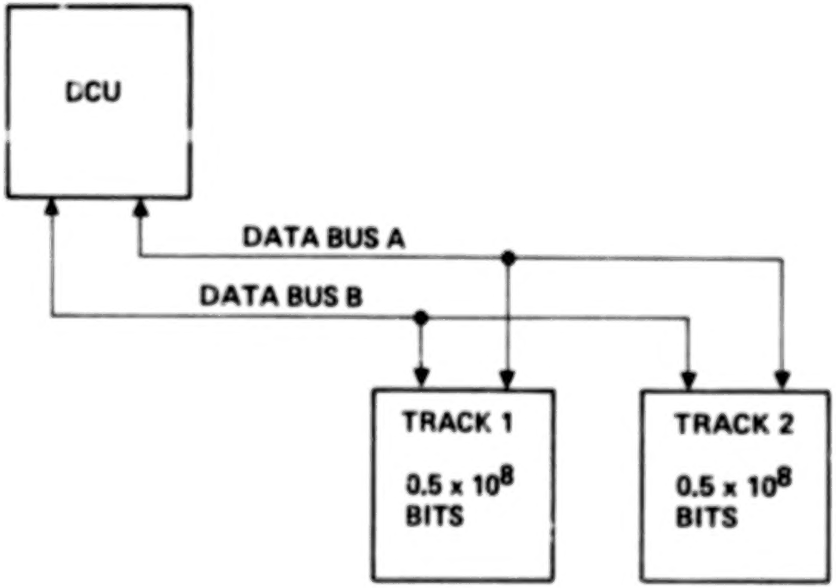
WEIGHT – 52.3 LB

MAX DATA RATE – 2.4 MHz

DSS SINGLE POINT FAILURE SUSCEPTIBILITY – 25% OF CAPACITY

PARTS COUNT – 3731

Figure 3-10. Model 1 DSS Configuration


DCU
DATA BUS A
DATA BUS B
TRACK 1
0.5 x 10^8 BITS
TRACK 2
0.5 x 10^8 BITS

CHARACTERISTICS

CAPACITY – 10^8 BITS

VOLUME – 598 IN^3

WEIGHT – 40.0 LB

MAX DATA RATE – 1.8 MHz

DSS SINGLE POINT FAILURE SUSCEPTIBILITY – 50% OF CAPACITY

PARTS COUNT – 2885

Figure 3-11. Model 2 DSS Configuration

Model 3 - This system organization is designed to achieve SSDR mechanical goals at the expense of functional capability. Basically this system is implemented by eliminating one of the tracks from the Model 2 design. This results in a system which had half the capacity of the SSDR goal, a reduced data rate and relatively high susceptibility to totally disabling single point failures. Figure 3-12 illustrates this system.

The options were discussed with NASA-Langley Research Center and it was agreed that the two track DSS configuration represented the best overall compromise in meeting the design goals for the SSDR. Based on this, a DSS configuration consisting of two memory tracks as illustrated in Figure 3-13 was selected for the final SSDR design.

3.4 FINAL SSDR SYSTEM DESIGN

Based on the considerations and tradeoffs described in the previous sections, a final SSDR organization was established as is illustrated in Figure 3-14. The following describes this organization and the resulting operational characteristics of the final SSDR system configuration. Allowable operating modes for this design are summarized in Table 3-4. Estimated physical parameters of this system prior to detail design were as given in Table 3-5. A brief description of the structure and operation of this organization follows.

Major block level components of the SSDR include four data buffers, four microprocessor based channel controllers, two bus controllers and two memory tracks. Data to or from either memory track may be transferred between the DSS and DCU over either of the two four bit wide bidirectional data buses (designated A and B). For a write operation, data is entered into the FIFO data buffer associated with the channel being used. The channel controller monitors status of the FIFO buffer and when the buffer is half filled, requests access to a data bus. After obtaining use of the data bus, the controller addresses the memory track and memory cell corresponding to the channel and current record location within the channel using the module controller associated with the allocated data bus. Under channel controller direction, the module controller generates the timing sequences required to write data into the addressed cell. The data is transferred to the memory track at 600K four bit bytes/sec. Internally in the memory module, this data is converted to sixteen bit bytes and written in parallel into the sixteen memory elements at the rotating field rate of 150 KHz. This transfer operation continues until the data buffer is empty or another channel controller requests the bus. The use of a FIFO for the data buffer allows the SSDR input data and internal transfer to the memory module to be asynchronous. As the addressed memory cell is filled, the controller maintains the cell's status, and when it is filled will sequence the cell address to the next cell allocated to the channel.

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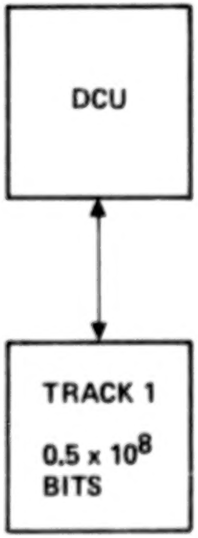
DCU
TRACK 1
0.5 x 10^8 BITS

CHARACTERISTICS

CAPACITY – 0.5×10^8 BITS

VOLUME – 393 IN^3

WEIGHT – 27.5 LB

MAX DATA RATE – 1.8 MHz

DSS SINGLE POINT FAILURE SUSCEPTIBILITY – 100% OF CAPACITY

PARTS COUNT – 1674

Figure 3-12. Model 3 DSS Configuration

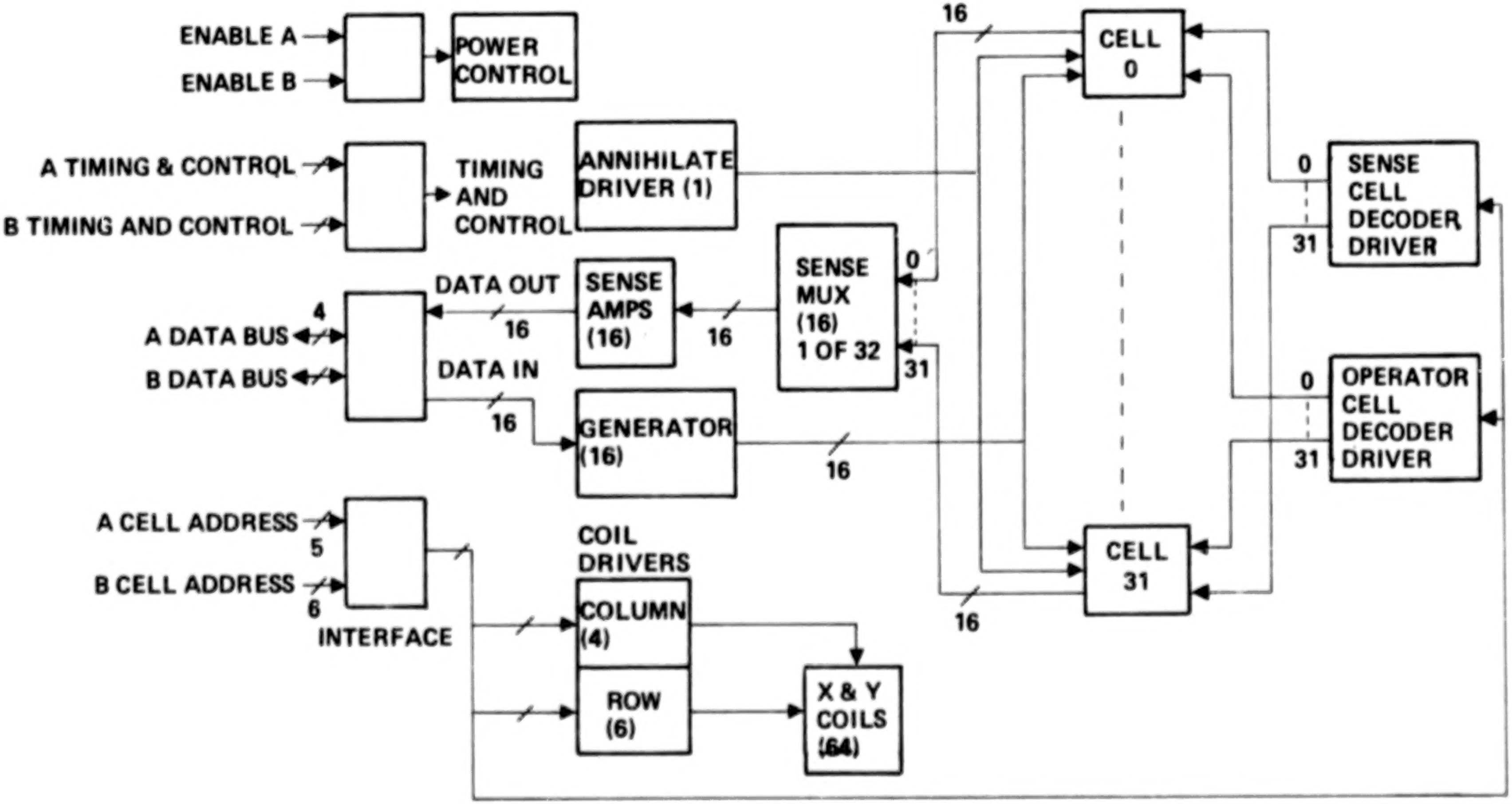
ENABLE A
ENABLE B
POWER CONTROL
A TIMING & CONTROL
B TIMING AND CONTROL
TIMING AND CONTROL
ANNIHILATE DRIVER (1)
DATA OUT
SENSE AMPS (16)
16
16
SENSE MUX (16) 1 OF 32
0
31
4
A DATA BUS
B DATA BUS
DATA IN
16
GENERATOR (16)
16
A CELL ADDRESS
5
B CELL ADDRESS
6
INTERFACE
COIL DRIVERS
COLUMN (4)
ROW (6)
X & Y COILS (64)
16
CELL 0
CELL 31
16
0
31
SENSE CELL DECODER DRIVER
0
31
OPERATOR CELL DECODER DRIVER

Figure 3-13. DSS Track Configuration

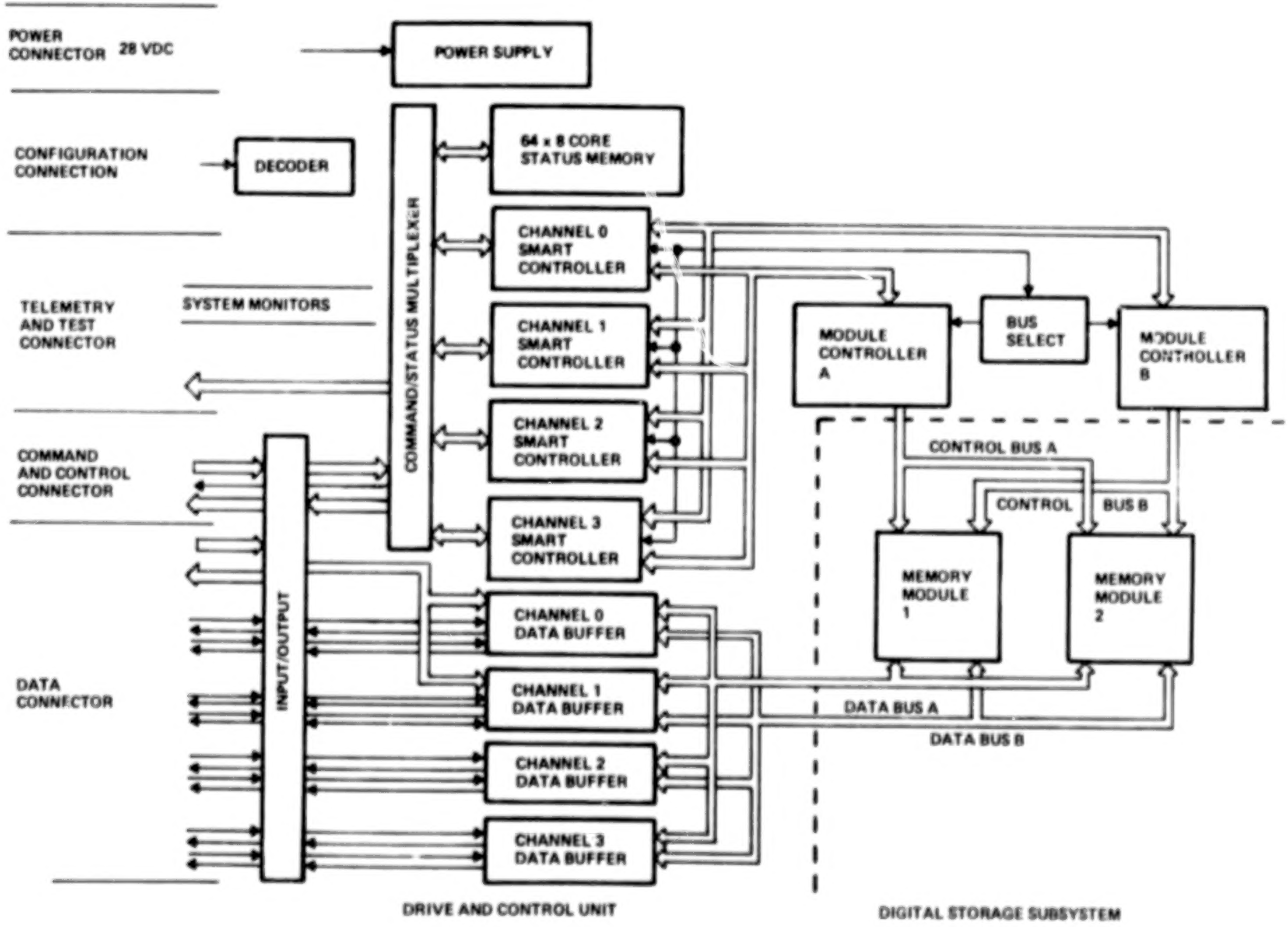
POWER CONNECTOR
28 VDC
POWER SUPPLY
CONFIGURATION CONNECTION
DECODER
64 x 8 CORE STATUS MEMORY
COMMAND/STATUS MULTIPLEXER
CHANNEL 0 SMART CONTROLLER
CHANNEL 1 SMART CONTROLLER
CHANNEL 2 SMART CONTROLLER
CHANNEL 3 SMART CONTROLLER
TELEMETRY AND TEST CONNECTOR
SYSTEM MONITORS
COMMAND AND CONTROL CONNECTOR
DATA CONNECTOR
INPUT/OUTPUT
CHANNEL 0 DATA BUFFER
CHANNEL 1 DATA BUFFER
CHANNEL 2 DATA BUFFER
CHANNEL 3 DATA BUFFER
MODULE CONTROLLER A
BUS SELECT
MODULE CONTROLLER B
CONTROL BUS A
CONTROL
BUS B
MEMORY MODULE 1
MEMORY MODULE 2
DATA BUS A
DATA BUS B
DRIVE AND CONTROL UNIT
DIGITAL STORAGE SUBSYSTEM

Figure 3-14. Solid State Spacecraft Data Recorder Final Configuration

Table 3-4. SSDR Configurations

Number of Channels	Interface	Channel Capacity	Transfer Per Channel	Rate Maximum Composite
1	8 Bit Parallel (1 Byte Serial)	100 M Bit (12.5 M Byte)	0 to 2.4 M Bit (0 to 150 K Byte)	2.4 M Bit
1	1 Bit Serial	100 M Bit	0 to 1.2 M Bit	1.2 M Bit
2	1 Bit Serial	50 M Bit	0 to 1.2 M Bit	2.4 M Bit
4	1 Bit Serial	25 M Bit	0 to 1.2 M Bit	<2.4 M Bit

Table 3-5. SSDR Physical Parameters

	Width In.	Length In.	Height In.	Volume In.^{3}	Weight Lb
SSDR	12.4	13.0	3.82	615.8	40.0
DSS	12.4	13.0	2.2	354.6	27.2
Memory Module	12.4	13.0	1.1	177.3	13.6
DCU	12.4	13.0	0.6	96.7	5.4
Miscellaneous	-	-	-	-	1.1
Power Supply, IO	12.4	13.0	1.0	161.2	6.3
Foot Print	13.4	14.0	3.9	731.6	-

A read operation is initiated by the channel controller of the commanded channel requesting a data bus. When the data bus (A or B) becomes available, the channel controller will instruct the module controller to address the track and cell associated with the channel and its current record location. Timing is then applied to the track from the module controller-causing data to be delivered from the addressed cell at 150,000 sixteen bit byes/sec. This data is converted to four bit bytes at 600K bytes/sec and transferred to the selected channels data buffer. The transfer continues until the data buffer is filled, another controller requests the bus or the channel read command is removed. When a cell is read, the channel controller will sequence to the next cell assigned to the channel maintaining the data flow. As with a write operation, the FIFO data buffer allows the internal SSDR data transfer to be asynchronous from the user read data rate.

Eight bit byte parallel read or write operation is achieved by using channel 0 and channel 1 controllers and data buffers. Four bits of each byte go to each of the two channels. The data from one channel is stored in track 1 and the data from the other in track 2. This allows both channels to operate in parallel giving a net data rate of 2.4 Mb/s.

A small core memory is used in conjunction with the channel controllers to maintain status information when the SSDR is powered down. Included in this status is such data as configuration and record status within each of the configured channels. This allows the SSDR to be reduced to a zero power state and still operate in an undisrupted manner when power is reapplied.

4.0 MEMORY CELL DESIGN

4.1 INTRODUCTION

The Memory Cell is the basic building block for a Bubble Memory system. It consists of the bubble memory elements, substrates for mounting and interconnection of the memory elements, coils for generating the rotating fields which drive the memory elements and a magnetic circuit which provides a bias field normal to the memory elements which is required for operation. Cell design presents a major challenge in terms of magnetic, mechanical and circuit design concepts. With a large memory system such as the SSDR is, the basic memory medium (in this case the memory cell) comprises a significant part of the total memory weight and volume. Thus the cell must be designed to minimize these parameters but to do so in a manner which will not adversely impact memory element margins or operating conditions.

In describing the design of the SSDR Memory Cell, a number of areas will be addressed. Major topics in this section will be comprised of a description of the memory element, conceptual cell design, detail magnetic design of the cell and detail mechanical design of the cell.

4.2 MEMORY ELEMENT

The memory element used on this program is a design designated M1067B. This device was developed on a prior program[1] and represents the results of a number of tradeoffs and iterations directed toward designing a memory element for applications such as the SSDR. The memory element has a storage capacity of 102,400 bits organized as a first-in/first-out serial memory. The chip has an area of 40.3 mm^3 (0.0625 in^2) with dimensions of 6.35 mm (.250 in.) per side. Fabrication of the memory element is accomplished by deposition of a $(YSm)_3\ (FeGa)_5\ O_{12}$ film on a 0.02" thick nonmagnetic garnet substrate using liquid phase epitaxy (LPE). The film properties are controlled such that a stable bubble diameter of 4 μm is obtained. Typical characteristics of the device material are summarized in Table 4-1.

---

[1] NASA Contract NAS1-12981 (See NASA CR-144983.)

Table 4-1 Typical Characteristics of Device Material

$4\pi M$ G.	W μm	H_{COL} oe.	H_{SO} oe.	σW Ergs/CM	η μM	ℓ μM	α
234	3.6	107.5	83.5	0.19	3.1	0.43	5

Fabrication of the device is done on two inch wafers using a two level process requiring three mask/photolithographic operations. The fabrication sequence involves the LPE growth of the magnetic garnet film, deposition of an SiO_2 spacer which is then covered with a Aℓ-Cu conductor layer. This conductor layer is etched to form the generator and annihilator components of the memory element. After these conductor paths have been formed, another space layer is deposited and a layer of permalloy is deposited on it. The permalloy is then masked and etched to form the propagation pattern and detector of the memory element. As a final step, the chip is masked to allow the second SiO_2 layer to be removed from the lower conductor layer at the bonding pad sites. Table 4-2 summarizes these various process steps used to form the memory element.

Table 4-2. Device Processing Sequence

Step No.	Thickness Å	Material/Function	Technique
1	900	SiO_2 Spacer	RF Sputter
2	4,500	Aℓ-Cu Conductor	Electron Beam Evaporation
3	15,000	AZ1350J Conductor Pattern	Standard Photolithography
4	--	Chemical Etch Aℓ-Cu	Immersion
5	6,000	SiO_2 Spacer	RF Sputter
6	3,500	Permalloy Propagate	RF Sputter
7	15,000	AZ1350J Propagate Pattern	Standard Photolithography
8	--	Ion-Etch Permalloy	VEECO Microetch
9	15,000	AZ1350J Oxide Pattern	Standard Photolithography
10	--	Chemical Etch SiO_2	Immersion

A schematic representation of the chip organization is illustrated in Figure 4-1. Data is contained in the closed storage loop area which is 102,400 bits long. As data is circulated in the storage loop, the passive replicator (which requires no external control signal) duplicates the data and steers it into the detector track where it is sensed by magnetoresistive effect. A dummy detector identical in structure to the active one is used to null out detector noise by sensing differentially across the active and dummy detectors. Separate current driven annihilator and generator elements for erasing and writing data are provided for altering data in the memory element. Physical configuration of the generator, annihilator and detector are such that all three functions occur within the same drive field cycle for a given bit location within the data storage loop.

Figure 4-2 illustrates the actual physical implementation of the memory element in terms of its various components. The storage area consists of H-I bar permalloy propagation elements with input-output functions implemented using chevron elements. The detector track is designed to stretch the bubble to a width of 100 chevron elements to generate sufficient signal amplitude to permit adequate sensitivity for reliable data sensing. An additional identical detector bonding pad is placed adjacent to the dummy detector to provide a magnetic environment for the dummy detector identical to that of the active detector to maximize common mode rejection.

The conductor level which comprises the annihilator and generator elements bonding pads are aluminum copper. Detectors and detector bonding pads are of the same permalloy as the propagation elements.

Amplitude and timing values and tolerances associated with the operation of the memory element are important in establishing design criteria for the memory cell and memory module circuit design. Table 4-3 summarizes values and tolerances for the various chip operating parameters that were established as a basis for detail design.

4.3 MEMORY CELL CONCEPTUAL DESIGN

The memory cell fills two basic functions; first, it provides means for generating the bias field and rotating fields required to operate the memory element and second, it provides a package to physically mount and interconnect the memory elements. Primary considerations involved in developing a memory cell design concept include weight and volume packaging efficiency, cooling and maintainability. A view of a typical bubble memory cell is illustrated in Figure 4-3. The rotating field is generated by a pair of orthogonal coils wound around the substrate containing the memory element. A bias field is generated by permanent magnetics connected in series in a magnetic circuit consisting of the magnets, ferrite bias plates and permalloy bias shell. Coils and memory element substrate are placed in an air gap in this magnetic circuit with the magnetics adjusted to provide the required field in the gap.

One obvious characteristic of this cell configuration is the lack of direct access to the memory element substrate which is enclosed on both sides by the rotating field drive coils. This presents difficulty in getting interconnect lines out of the cell, poor cooling characteristics for the substrate and a complicated disassembly process if a memory element must be replaced.

Table 4-3. Memory Element Operating Requirements

	Amplitude		Width		Phase	
	Value	Tolerance	Value	Tolerance	Value	Tolerance
Operator Functions						
Generate	150 ma	±10%	140 ns	±5%	240°	±4%
Annihilate	110 ma	±10%	400 ns	±5%	195°	±5%
Field Functions						
Drive Field	55 oe	±10%				
Bias Margin		±3 oe				
Bias Temp Coeff	.2%/°C	±15%				
Holding Field	4.3 oe	±30%				
Center Bias Field	102.5 oe	±7.5 oe				
Detector Functions						
Resistance	550 Ω	±18%				
Dummy Active Mismatch	15 Ω Max					
Max Detector Current	15 ma					
Max "0" Signal	0.2 mv/ma					
Min "1" Signal	1.0 mv/ma					
Strobe Position	274°	±4°				
Clamp Release Position	232°	±5°				

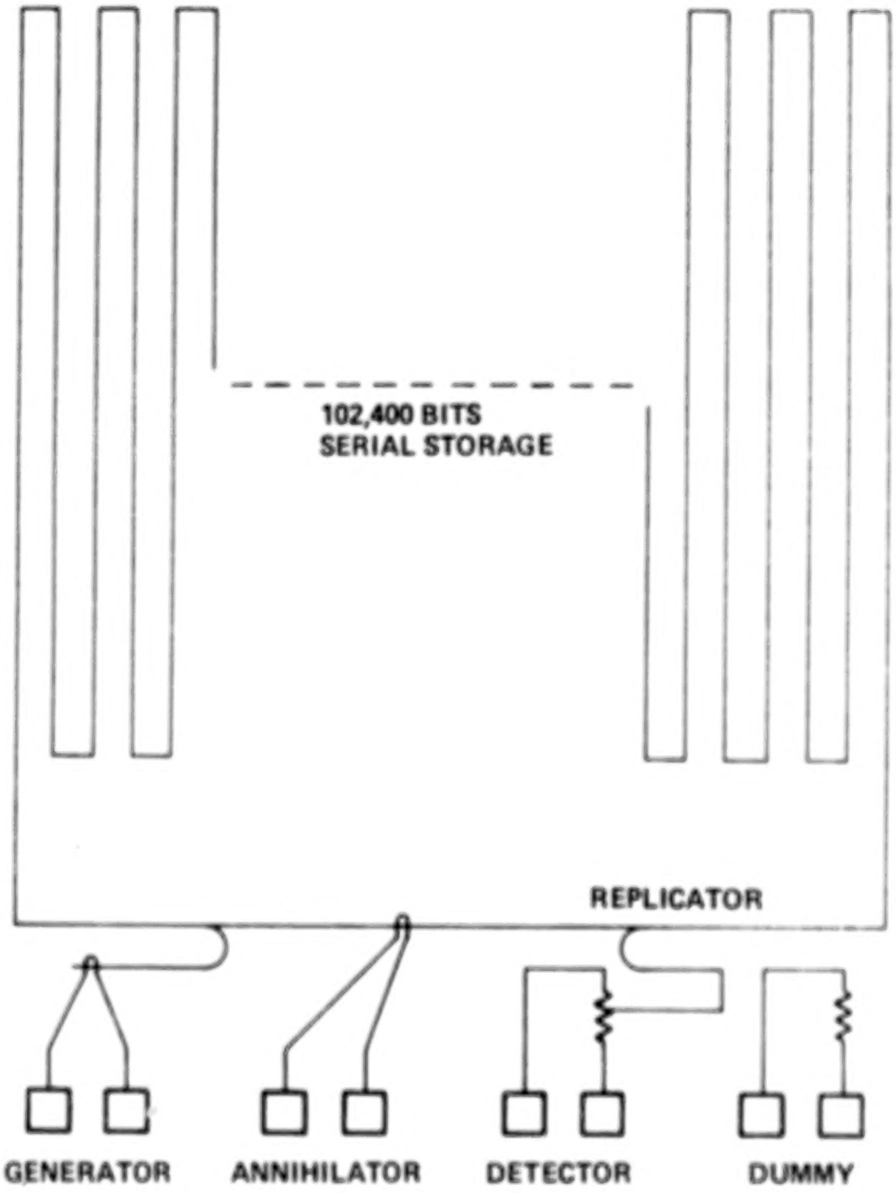
102,400 BITS
SERIAL STORAGE
REPLICATOR
GENERATOR
ANNIHILATOR
DETECTOR
DUMMY

FIGURE 4-1. 1067B MEMORY ELEMENT SCHEMATIC

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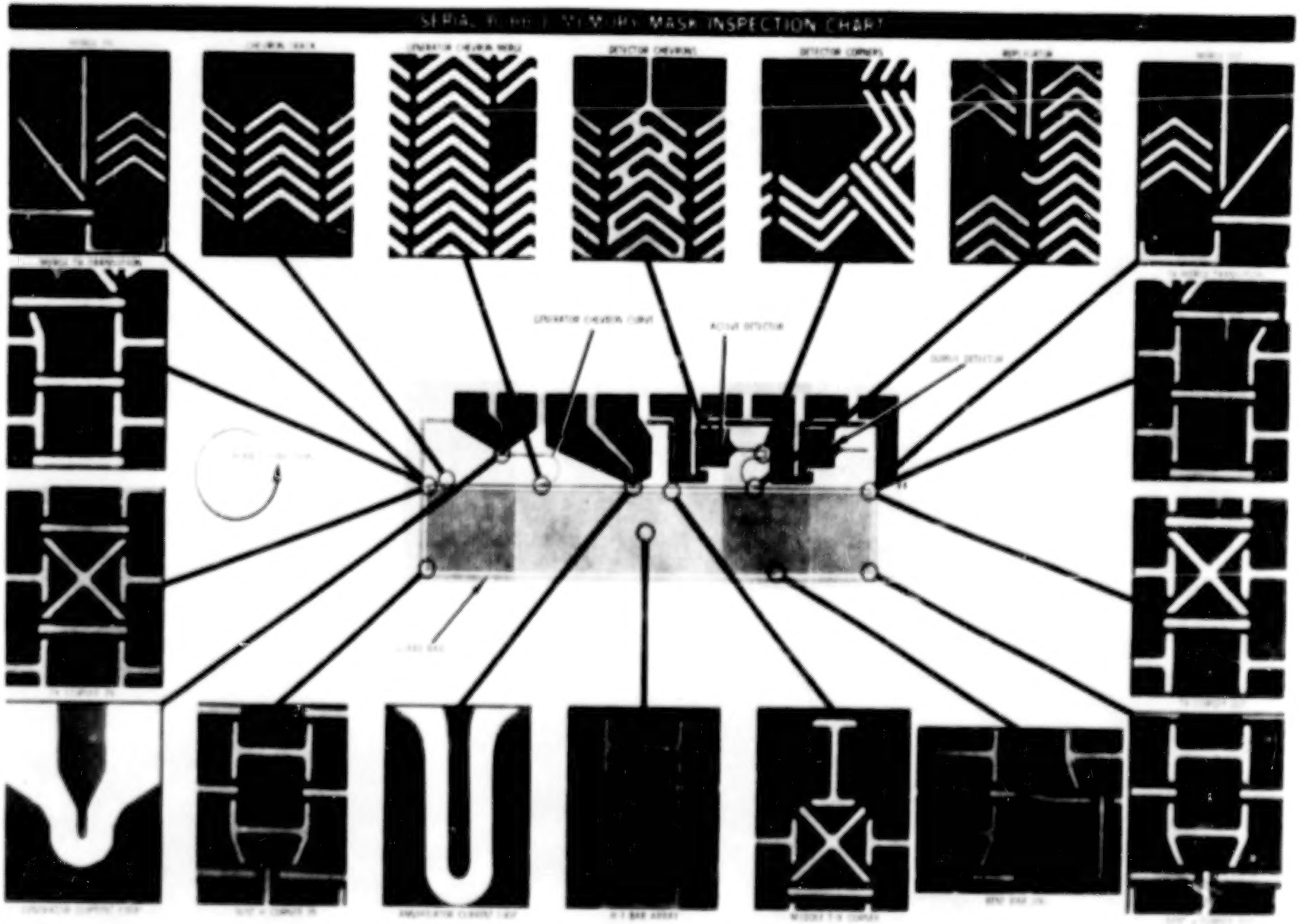
SERIAL BUBBLE MEMORY MASK INSPECTION CHART
CHEVRON TRACK
DETECTOR CHEVRONS
DETECTOR CORNERS
REPLICATOR
GENERATOR CHEVRON CURVE
ACTIVE DETECTOR
DUMMY DETECTOR

Fig 4-2. 1067B Memory Element Components

MICROFILMED FROM
BEST AVAILABLE COPY

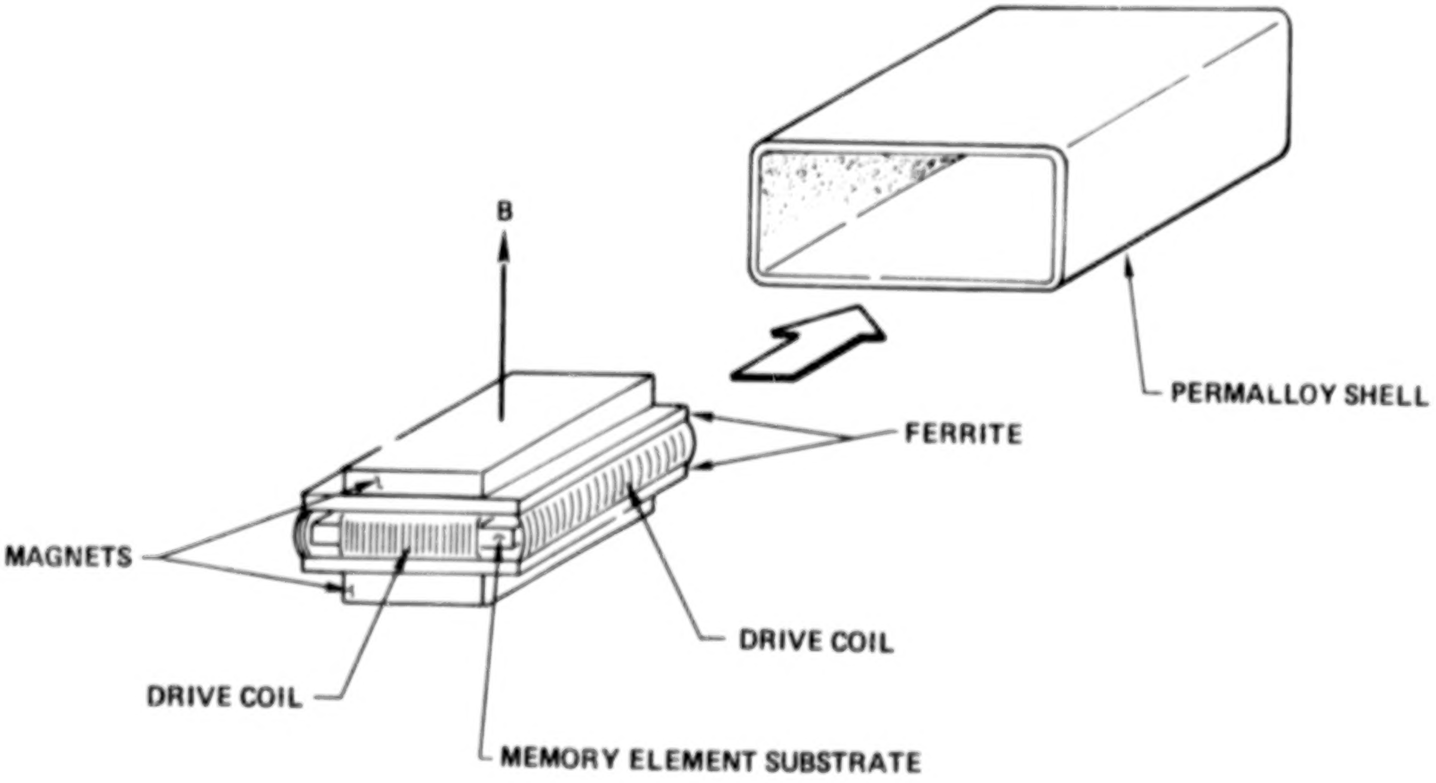
B
PERMALLOY SHELL
FERRITE
MAGNETS
DRIVE COIL
DRIVE COIL
MEMORY ELEMENT SUBSTRATE

FIGURE 4-3. CELL STRUCTURE

Because of this, an early ground rule established for cell design was the use of a concept which would allow direct access to the substrate for cooling, interconnect and repair. An additional objective was to package sufficient memory elements in a cell such that the weight and volume per bit of the cell tended toward a minimum value. The initial approach to achieving these goals involved use of a technique as illustrated in Figure 4-4. X and Y rotating field coils were wound orthogonally around a ferrite sheet and mounted to one inside surface of a rectangular copper structure with open ends. Memory elements would be mounted to the opposite inside surface allowing free access to the memory elements. The exposed X and Y coils on the ferrite sheet generate image currents in the copper that effectively make the chip mounting surface appear as if it were magnetically at the center of a closed X and Y coil with a height equal to twice that of the copper structure. Eight chips would be mounted in a structure and two such structures would be mounted in a bias assembly to form a basic cell.

In principle, this concept was functional. However, it was found that if the drive field had any average D.C. component, it would penetrate the copper structure, encounter the high permeability material of the bias assembly and result in a relatively large field normal to the chip which would cause an unacceptable modulation of the bias field. Because of this, an alternate approach to coil design was adopted. The basic concept for this design is illustrated in Figure 4-5. Access to the coil interior is gained by spreading the ends of one coil open such that both coils close in the same plane.

A second problem was encountered in the area of the bias structure. The original concept, as indicated previously, was to place two eight memory element coil sets in a single bias assembly to minimize weight and volume. This design is illustrated in Figure 4-6. It was intended that the bias for each cell would be individually adjusted by a variable shunt across the uniform field area in question. However, the interaction between bias field amplitude in the two coils was such that a single cell field value could not be adjusted without an iterative adjustment procedure involving both cells. Such a procedure was judged to be unacceptably complex. Because of this, it was decided that all sixteen memory elements would be matched to operate with the same bias field. This then leads naturally to combining the two eight chip substrates into a single coil set to further reduce cell weight and volume. This approach then represents the basis used for establishing the final detailed design of the memory cell.

4.4 MEMORY CELL MAGNETIC DESIGN

As discussed in previous sections, the memory cell must provide three magnetic fields required for memory element operation. These fields are the bias field, rotating field and holding field. A primary objective of the magnetic design was to ensure the correct value and uniformity of these fields. A second major concern relative to the rotating field is to establish the design details of the coil winding to minimize power dissipation and establish a coil impedance that is compatible with coil drive circuit design constraints.

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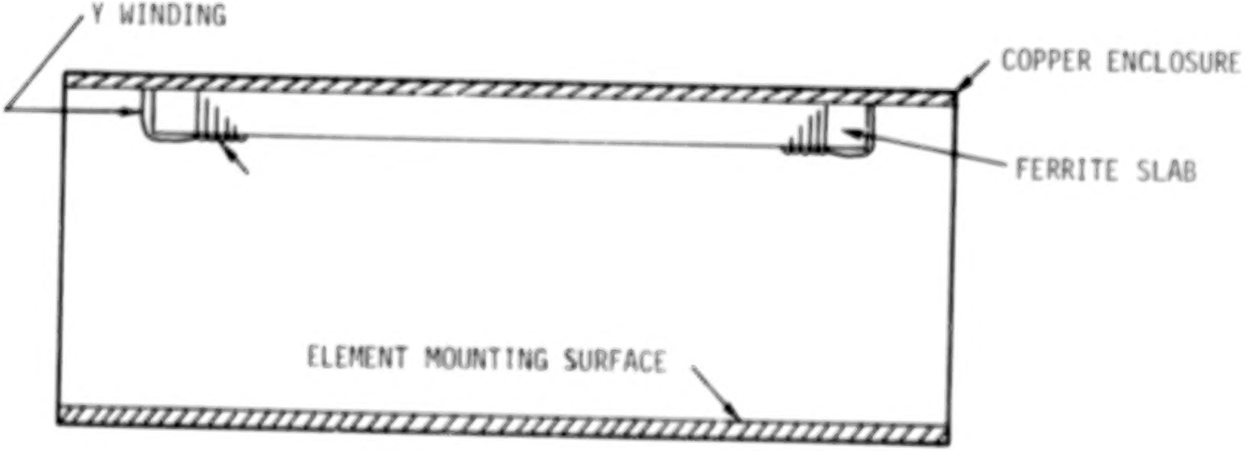
Y WINDING
COPPER ENCLOSURE
FERRITE SLAB
ELEMENT MOUNTING SURFACE

FIGURE 4-4. INITIAL COIL DESIGN

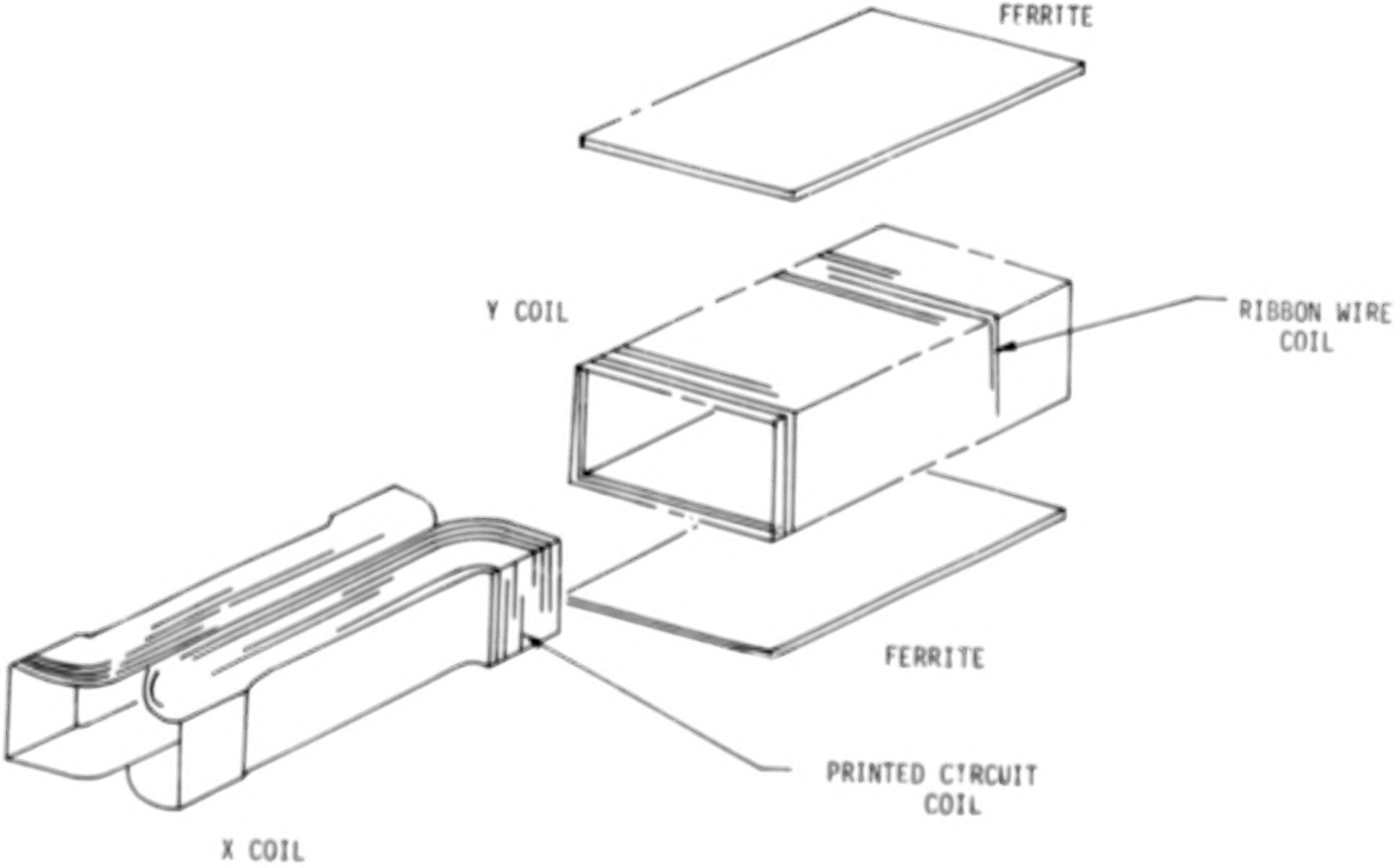
FERRITE
Y COIL
RIBBON WIRE COIL
FERRITE
PRINTED CIRCUIT COIL
X COIL

FIGURE 4-5. BASIC MEMORY COIL CONFIGURATION

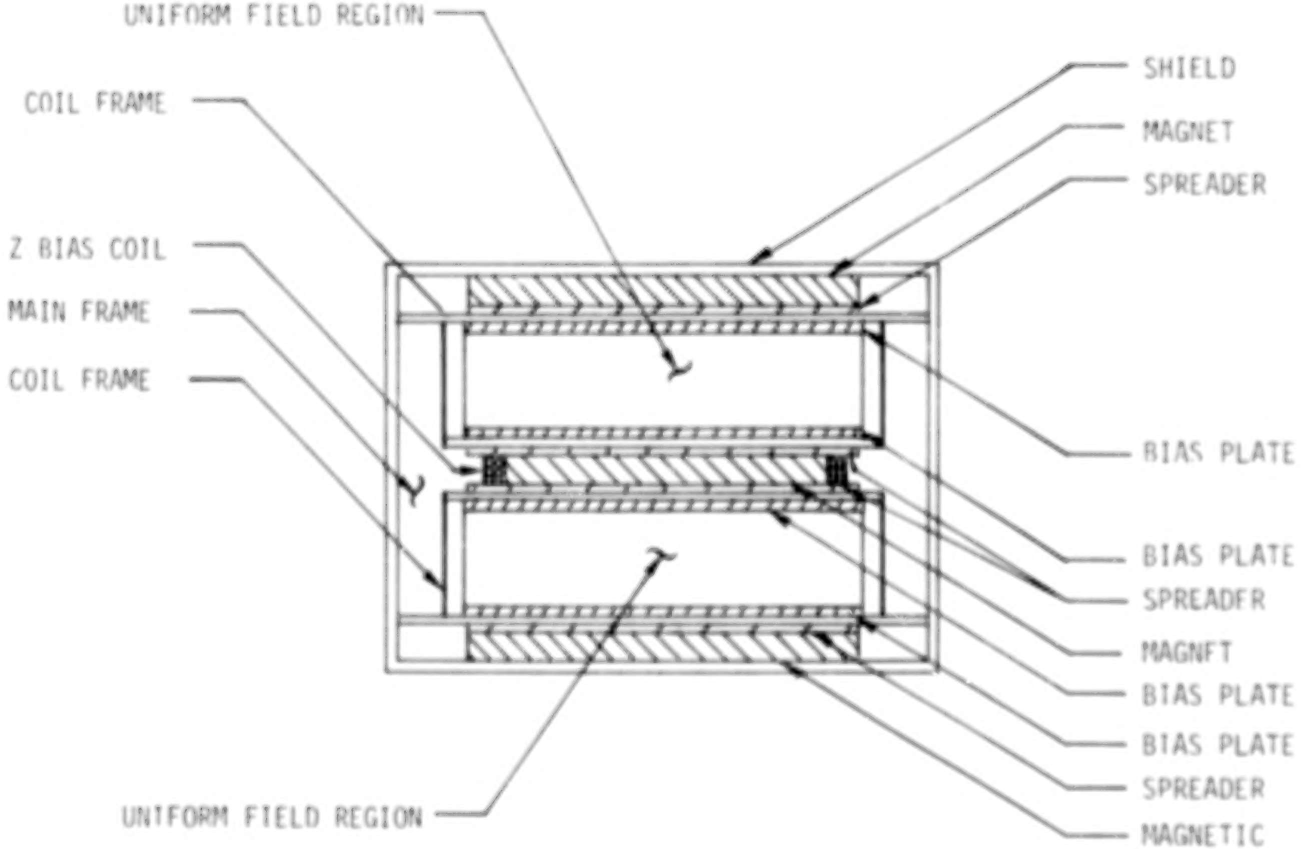
UNIFORM FIELD REGION
COIL FRAME
Z BIAS COIL
MAIN FRAME
COIL FRAME
UNIFORM FIELD REGION
SHIELD
MAGNET
SPREADER
BIAS PLATE
BIAS PLATE
SPREADER
MAGNET
BIAS PLATE
BIAS PLATE
SPREADER
MAGNETIC

FIGURE 4-6. TWO COIL BIAS ASSEMBLY SECTION

The cross section of Figure 4-7 illustrates the major elements of the cell magnetic design. The outer shell of the cell is made of permalloy and serves the dual function of providing a return path for the bias field flux and also serves to shield the memory elements from external magnetic fields. The bias area is located symetrically within the bias shell by placing magnets on both sides of the bias area. This makes the magnetic potential of the shell equal to that at the center of the bias area and minimizes distortion of the bias field caused by bias area to shell fringing. The bias magnets are divided into two parts to minimize lateral flux flow in the ferrite bias plates. The permanent magnets are barium ferrite which has a temperature coefficient that matches that of the bubble device and allows extended temperature operation of the cell.

The bias field is set for a cell by applying an external magnetic field of sufficient amplitude to saturate the bias shell and also saturate the permanent magnets. The applied field is then reversed and increased in amplitude sufficiently to reduce the magnetization of the permanet magnets sufficiently to produce the required bias field. This procedure produces the most stable bias field configuration[2]. A winding called a Z-coil is wound around one set of magnets (See Figure 4-7) to provide a means of electrically modulating the bias field for test purposes. Figure 4-8 illustrates data on the uniformity of the bias field generated by the SSDR bias structure design. As seen from this data, the bias field is uniform within 1% over the chip active area of the cell.

Design of the X and Y drive coils for the cell took into account field uniformity coil impedance and loss. The basic coil size was established to ensure that the rotating field amplitude was uniform within ten percent over the active chip area. Figures 4-9 and 4-10 illustrate data on X and Y field uniformity for the SSDR cell design. From these figures, it may be seen that field uniformity is held within 3% for both X and Y fields, leaving a total variation for voltage and circuit variations.

The details of the coil winding were selected to achieve lowest possible loss, correct coil impedance and proper sensitivity. Since the coil drive system selected (See Section 5.0) utilized a voltage switched drive, the X and Y coils were to have equal sensitivity in terms of oe/volt sec. Another limitation placed on the coil design was a maximum coil current of 3 amps at the required nominal operating field of 55 oe. This limit is based on semiconductor devices available for use in the coil drive circuit. Using these factors, the open X coil was designed for 40 turns/inch which resulted in a drive sensitivity of 920,333 oe/volt sec. and the wound Y coil had a 39 turn/in winding and a drive sensitivity of 876,700 oe/volt sec. providing X and Y drive sensitivity

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[2] "Relationship of Bias Field Setting Procedure to Field Stability Against External Field Perturbations for Magnetic Bubble Memory Bias Field Structures" W. J. DeBonte and R. Zapulla, IEEE Transation on Magnetics Mag 12, No. 6, November 1976.

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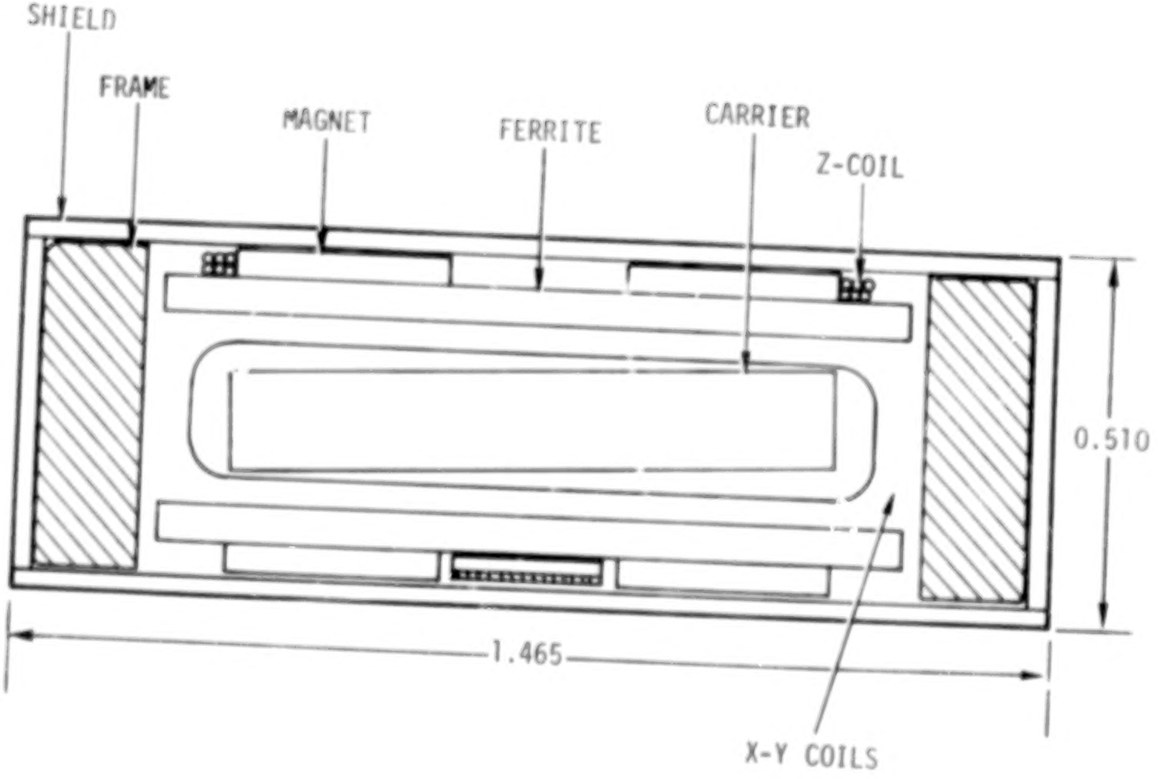

SHIELD
FRAME
MAGNET
FERRITE
CARRIER
Z-COIL
0.510
1.465
X-Y COILS

Fig 4-7. Cell Section

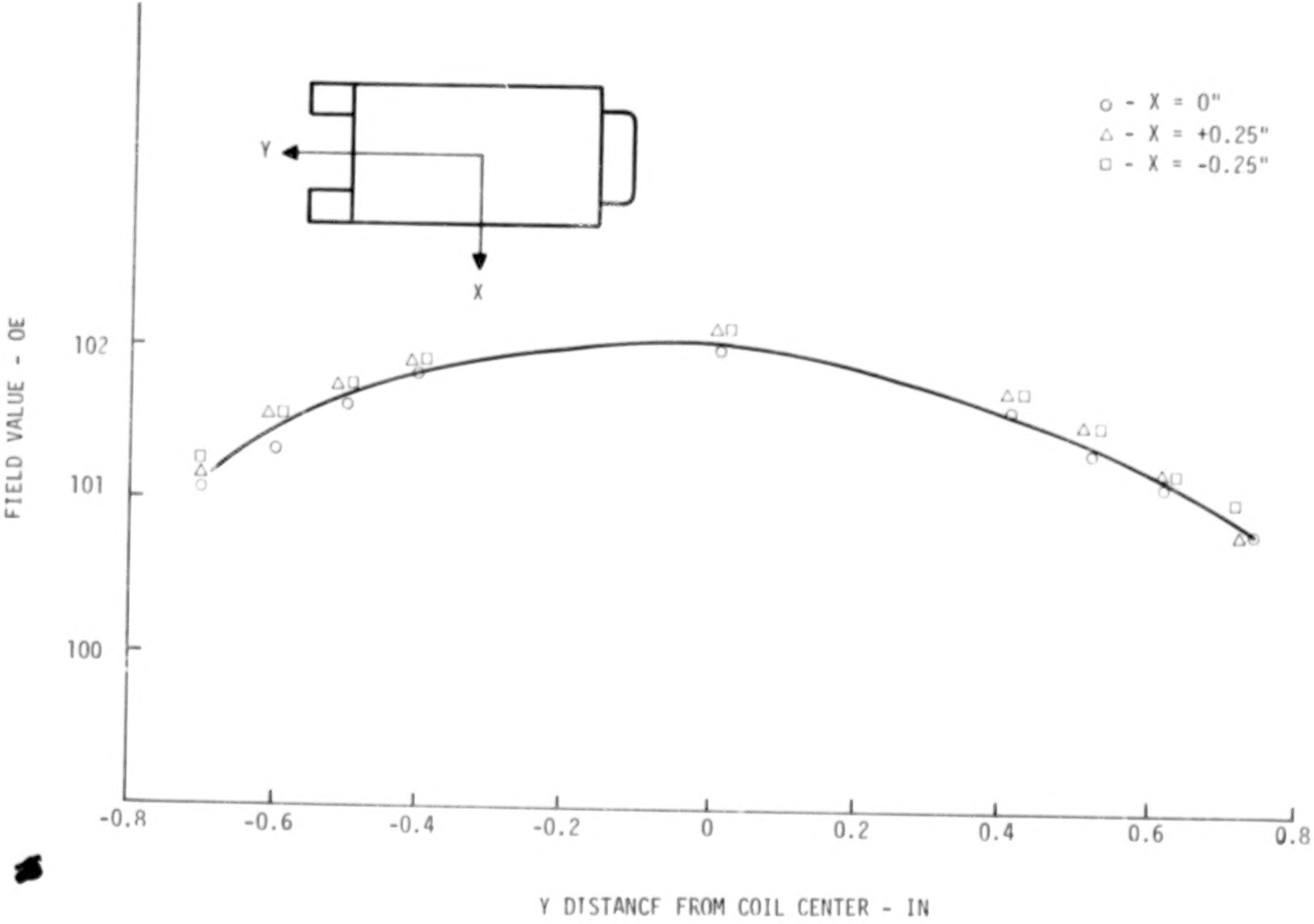


FIGURE 4-8. BIAS FIELD UNIFORMITY

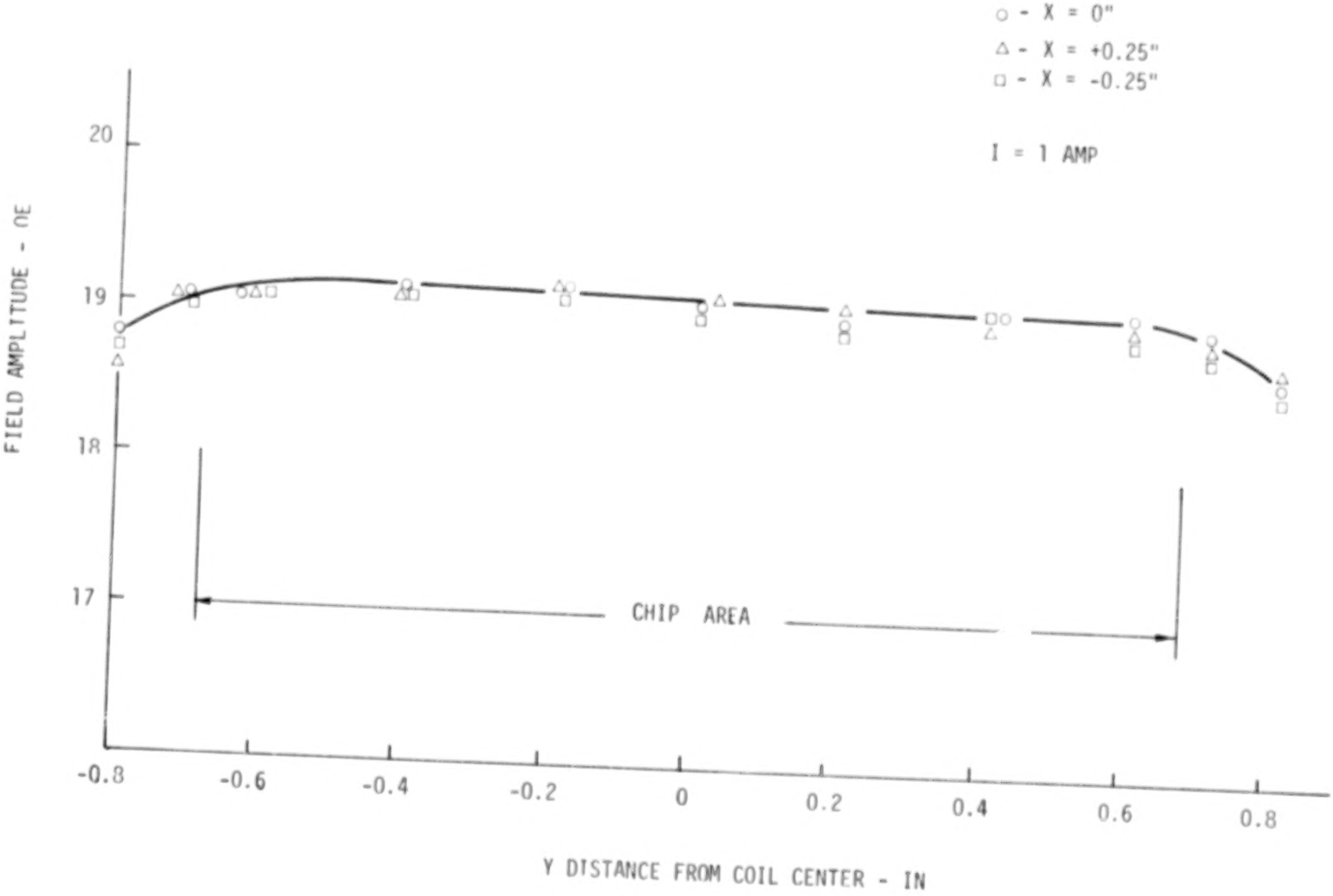


FIGURE 4-9. Y COIL FIELD UNIFORMITY

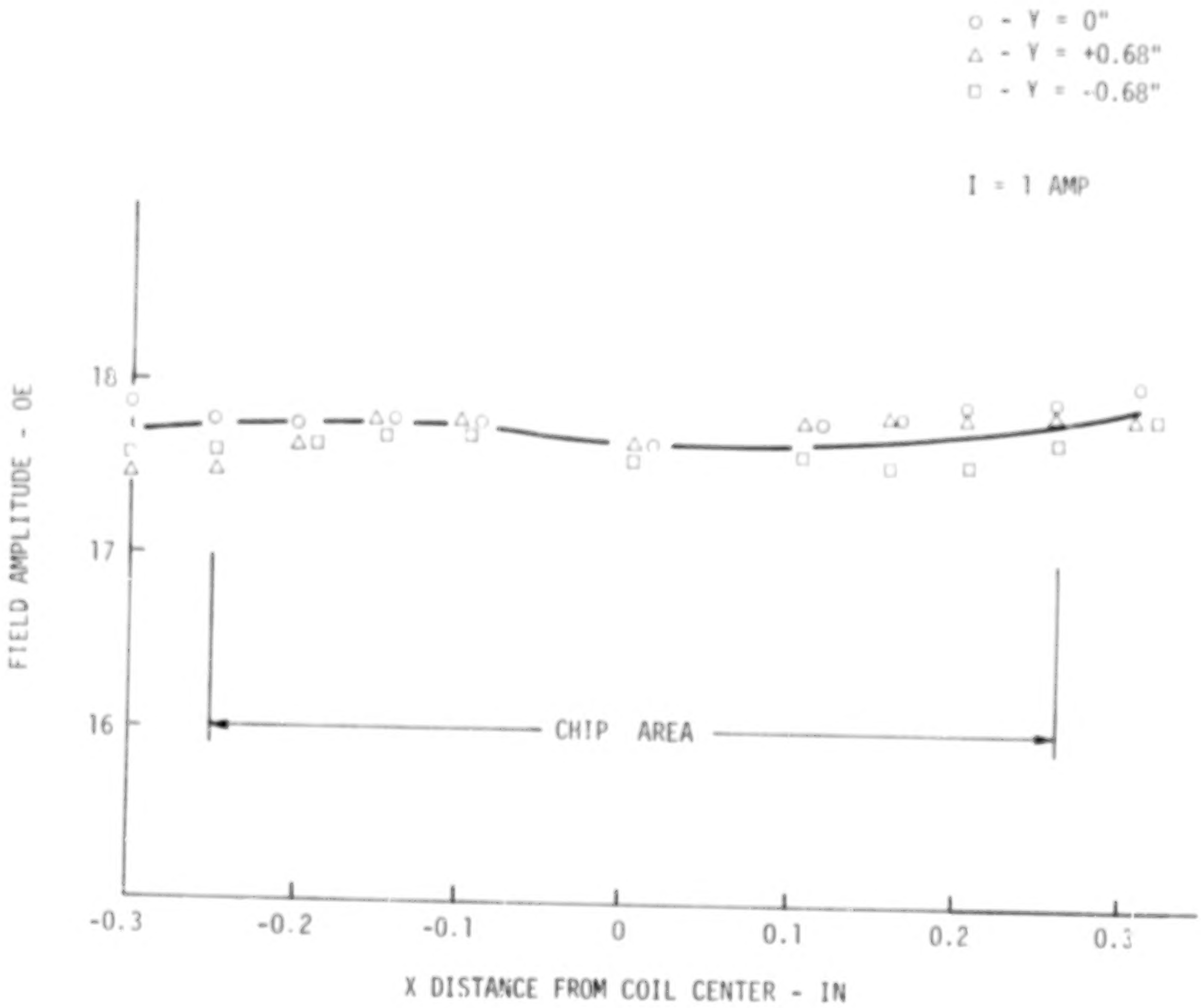


FIGURE 4-10. X COIL UNIFORMITY

matching within 5%. This resulted in X coil terminal characteristics of 19 μhy in series with 1.5 ohms at the operating frequency of 150 KHz. Y coil terminal characteristics were 21 μhy in series with 0.95Ω.

Both windings were implemented using rectangular conductors. The open X coil was implemented using an etched flexible circuit while the wound Y coil used rectangular wire. Rectangular wire was chosen for the wound coil since it provides more copper conductor per turn than round wire and hence a lower resistance. Wire thickness was specified at the optimum value for the operating frequency of the coil which is about 1.55 skin depths. This resulted in a wound Y coil using two layers of 25 mil x 6 mil wire connected in parallel and a flex circuit X coil consisting of two 5 mil x 20 mil circuits connected in parallel.

A final consideration in magnetic design of the memory cell is the need for a holding field in the plane of the memory elements. This field is required to maintain a magnetic polarization of the permalloy propagation elements on the bubble chips when the rotating field is turned off. Without this field, minimum energy locations for the bubbles are not well defined and errors may result during start-stop operations. This field is generated by tilting the memory element substrates in the bias field as illustrated in Figure 4-7. This results in a component of the bias field in the plane of the memory element to generate the required holding field. However, this then presents a problem with the rotating field since there will now be a component of this field normal to the chip which will modulate the bias field causing bias field margin degradation. To avoid this problem, each of the two substrates in the cell is sandwiched between two 4 mil sheets of copper. These copper sheets act as eddy current shields to the chip normal component of the rotating field and effectively remove this field from the chip area. These copper sheets are grounded and serve the secondary function of acting as an electrostatic shield between the high coil voltages and low level sense signals on the substrates.

4.5 MEMORY ELEMENT SUBSTRATE LAYOUT

As discussed previously, the memory cell contains two substrates of eight memory elements each. These substrates are of a thick film ceramic type which provide the interconnect to get the sense signals out of the cell. Because of the high voltages and magnetic fields associated with the rotating field, great care must be taken in layout to ensure an acceptable signal to noise ratio. The environment faced in this problem includes magnetic fields on the order of 50 oe and voltage transitions of 60 volts with harmonics in the MHz region. The two major problems associated with this environment are: 1) $D\phi/dt$ noise and 2) cross-coupled currents. Strategies used in minimizing these problems in substrate layout are described in the following sections.

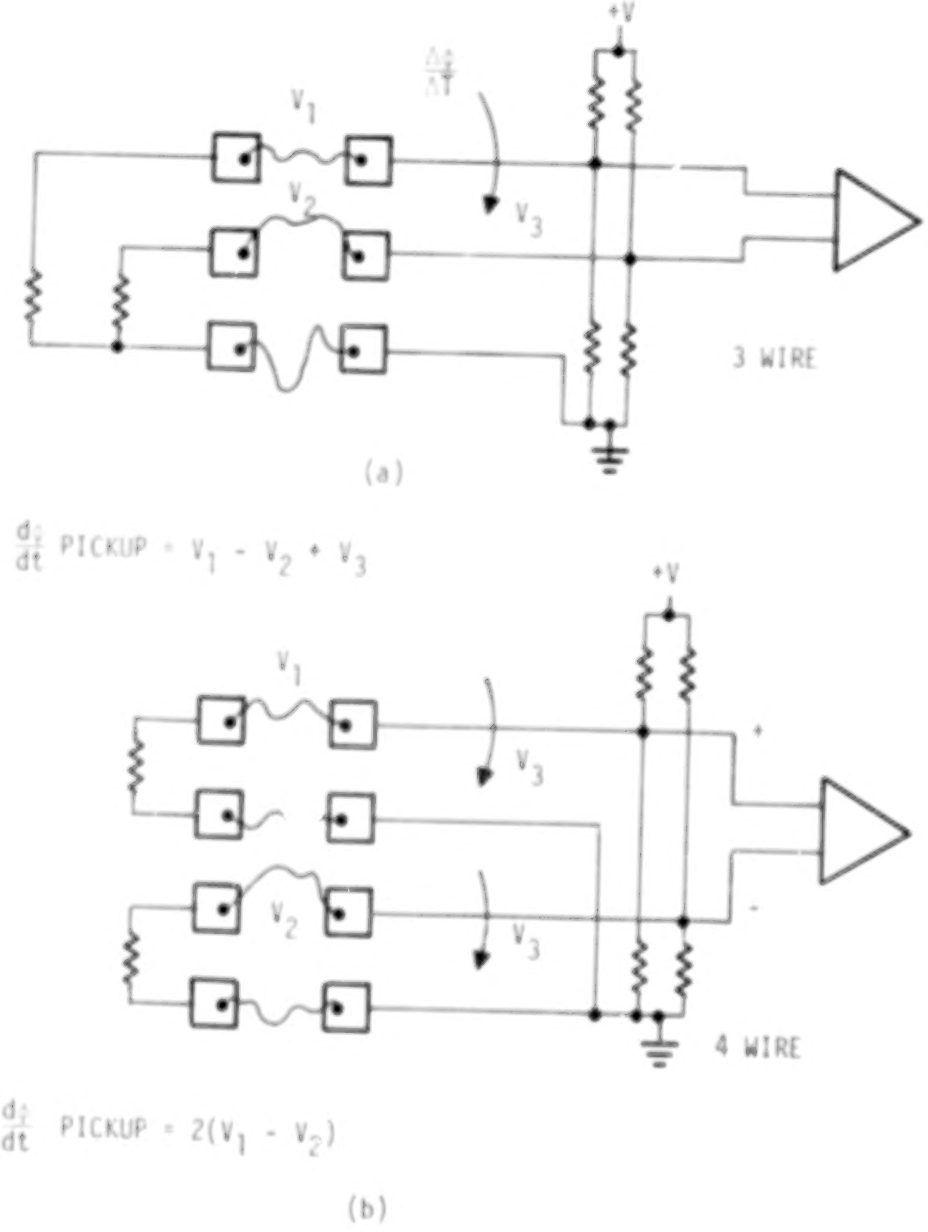
4.5.1 Dϕ/DT Noise

This noise is a voltage which is induced in a loop of conductor whose cross section is exposed to the rotating field. The loop area, the frequency or risetime, the magnitude of the field, and the orientation of the field with respect to the loop all influence the magnitude of the noise. Because of the potential noise problem due to chip bonding and the long substrate conductor runs an approach of tight bonding control and a four wire conductor scheme were adopted. Figure 4-11(b) shows a four wire detector connection where the pickup in the two loops cancel in a uniform field. This is better than the three wire connection shown in Figure 4-11(a) for those designs where the conductor runs are long and where the chip to substrate bonds are well controlled. For the four wire system, the net sense leads are nearly negligible primarily because two closely spaced, independent, nearly identical, self-cancelling loops egress from the package and are connected outside the field area. Dϕ/dt induced in one loop will nearly cancel with the dϕ/dt induced in the other loop.

To make the potential difference as small as possible, the conductor-to-conductor spacing was the practical minimum for the ceramic boards. The connection of the ground of the two loops was made outside of the field area where the field magnitude is less than 10% of the center field. A second area in which noise may be coupled into the sense loop is through the loop formed by the vertical run of bonds from detector and dummy to substrate surface. To minimize this source of noise, care is taken in the bonding process to ensure the area enclosed by dummy detector bonds is equal to the area enclosed by the active detector bonds. Under these conditions, the induced noise will cancel out in a four wire system.

4.5.2 Cross-Coupled Currents

When current is driven into a coil a voltage is produced in proportion to the coil's inductance. This voltage will cause currents to flow into the sense channel through coil to substrate capacitance. One purpose of using a differential line is to balance the coupled currents so that they are common mode into the sense line pairs and not detected. However, the lines must be carefully balanced to achieve this goal. An example is given in Figure 4-12 where a floating conductor is placed next to the balanced pair. About 10 millivolts of noise can be expected from the conductor if it floats but less than a millivolt if it is grounded so that the differential pair is effectively guarded. Another source of unbalance is tolerance of the conductors. A 10% difference in average width between active and dummy conductors will produce approximately 0.4 millivolts of noise at the fundamental frequency. The clamped and strobed sense channel will see 0.28 millivolts of this at the amplifier input. Conductor separation is of minor importance on the substrate compared to placement.


+V
$\frac{\Delta\phi}{\Delta T}$
V_1
V_2
V_3
3 WIRE
(a)
+V
V_1
V_3
+
V_2
V_3
-
4 WIRE
(b)

$\frac{d\phi}{dt}$ PICKUP = $V_1 - V_2 + V_3$

$\frac{d\phi}{dt}$ PICKUP = $2(V_1 - V_2)$

FIGURE 4-11. INDUCTIVE NOISE PICKUP

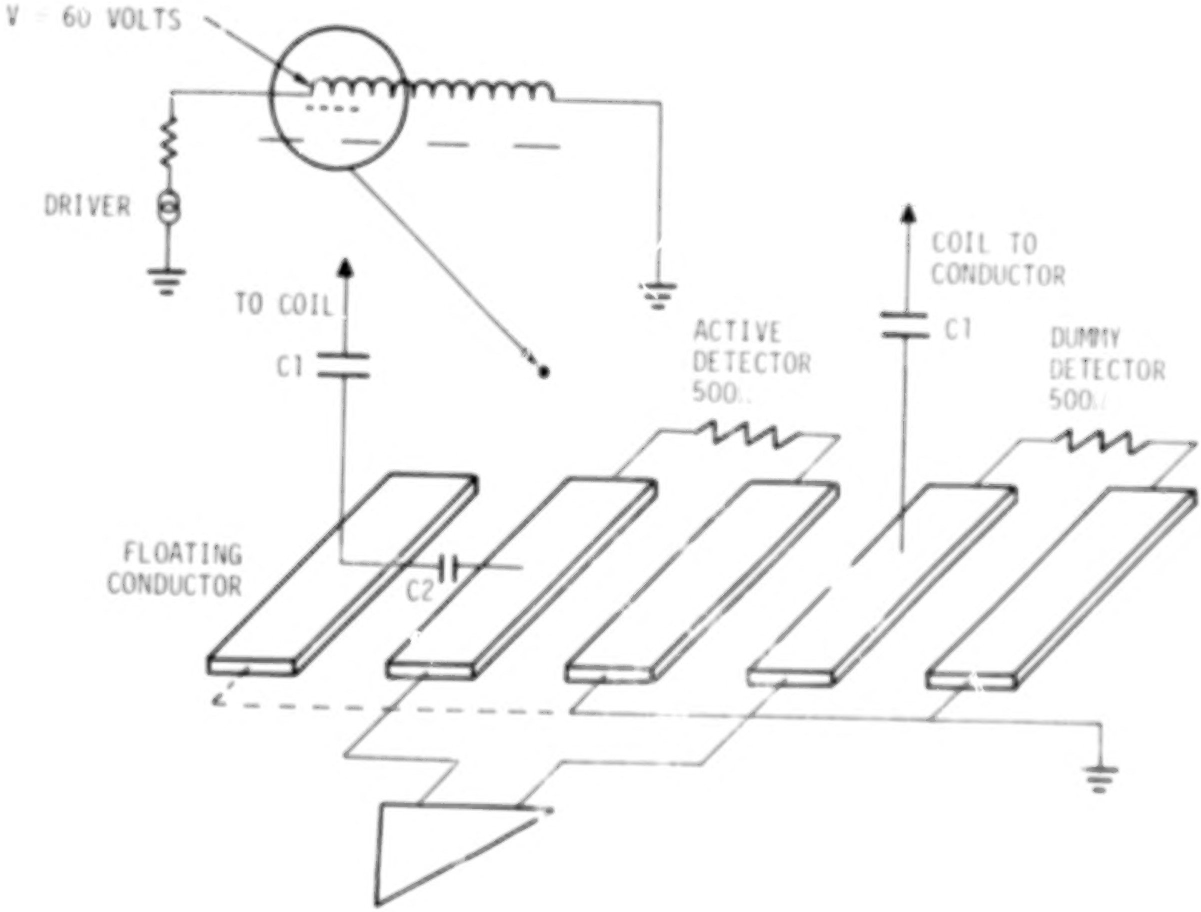

V = 60 VOLTS
DRIVER
TO COIL
C1
C2
FLOATING CONDUCTOR
ACTIVE DETECTOR 500Ω
COIL TO CONDUCTOR
C1
DUMMY DETECTOR 500Ω

FIGURE 4-12. CAPACITIVE NOISE PICKUP

4.6 CELL MECHANICAL DESIGN

The cell design developed for the SSDR contains sixteen 100K bit memory elements, weighs .28 lb. and has a volume of 2.23 in^3. Principle components of the cell include bubble chips, two ceramic chip carriers, X-Y rotating field coils, ferrite bias plates, ceramic magnets, Z perturb coil, permalloy shield keeper, aluminum frame and carrier securing hardware. Details of the cell are shown in the photographs of Figures 4-13 and 4-14.

4.6.1 Carrier

Referring to Figures 4-15 and 4-16, components of the carrier include 8 bubble chips, a ceramic Printed Wiring Board (PWB), aluminum and beryllium oxide spacer details, 26 beam lead diodes, a copper field alignment plate and a flexible interconnect cable. The carrier has a storage capacity of 8 x 10^5 bits, is .054 in. thick, .850 wide and 3.020 long.

The ceramic PWB has two layers of fired thick film gold conductors on one side of a ground aluminum oxide substrate .018 in. thick. Platinum gold metallization is utilized for pads associated with the flexible interconnect cable and copper plate solder terminations. Five mil wide conductors on 10 mil centers are used for detector circuits whereas wider metallization is required for high current operator circuits. PWB flatness is maintained through the metallization process by screening and firing compensating dielectric layers on the back side.

As shown in Figure 4-15, four aluminum oxide bars and one beryllium oxide plate are adhesively bonded to the circuit side of the metallized PWB. These details form a spacing window around the chip mounting area, increase the stiffness of the carrier and are lapped flat in assembly to provide a precision mechanical and thermal interface. The beryllium oxide plate is used to minimize the thermal resistance to one end of the chip field. Three carrier mounting holes are drilled through the beryllium oxide plate and aluminum oxide substrate prior to assembly.

Twenty-six beam lead diodes for sense matrixing are pulse thermcompression bonded to pads in the area shown in Figure 4-15. A 4 mil thick rolled and annealed insulated copper plate is adhesively bonded to the back of the PWB and is grounded via a soldered tab which passes through a fourth hole in the PWB. This plate is utilized to planarize the rotating magnetic field and shield the PWB circuitry from voltage induced noise.

Eight bubble chips are aligned and adhesively bonded active side up to sites fired onto the PWB surface. Adhesive coated .5 mil mylar preforms are bonded over the active surface of the chips and are utilized to space away magnetic foreign materials which are found to interfere with bubble propagation. The bubble chip detectors are interconnected using 1 x 3 mil aluminum ribbons which are terminated using an ultrasonic bonding process.

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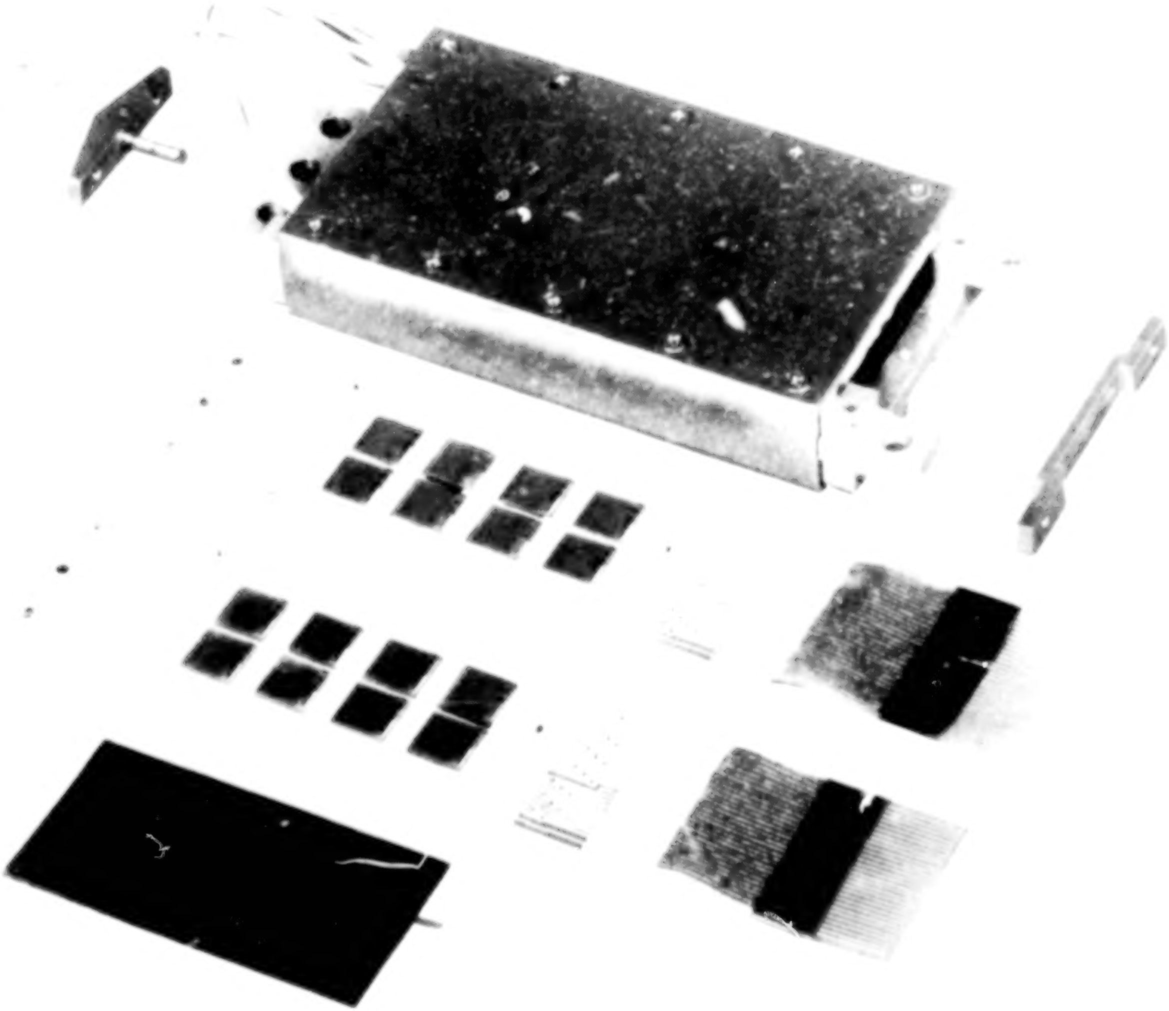

Fig 4-13. Cell Components

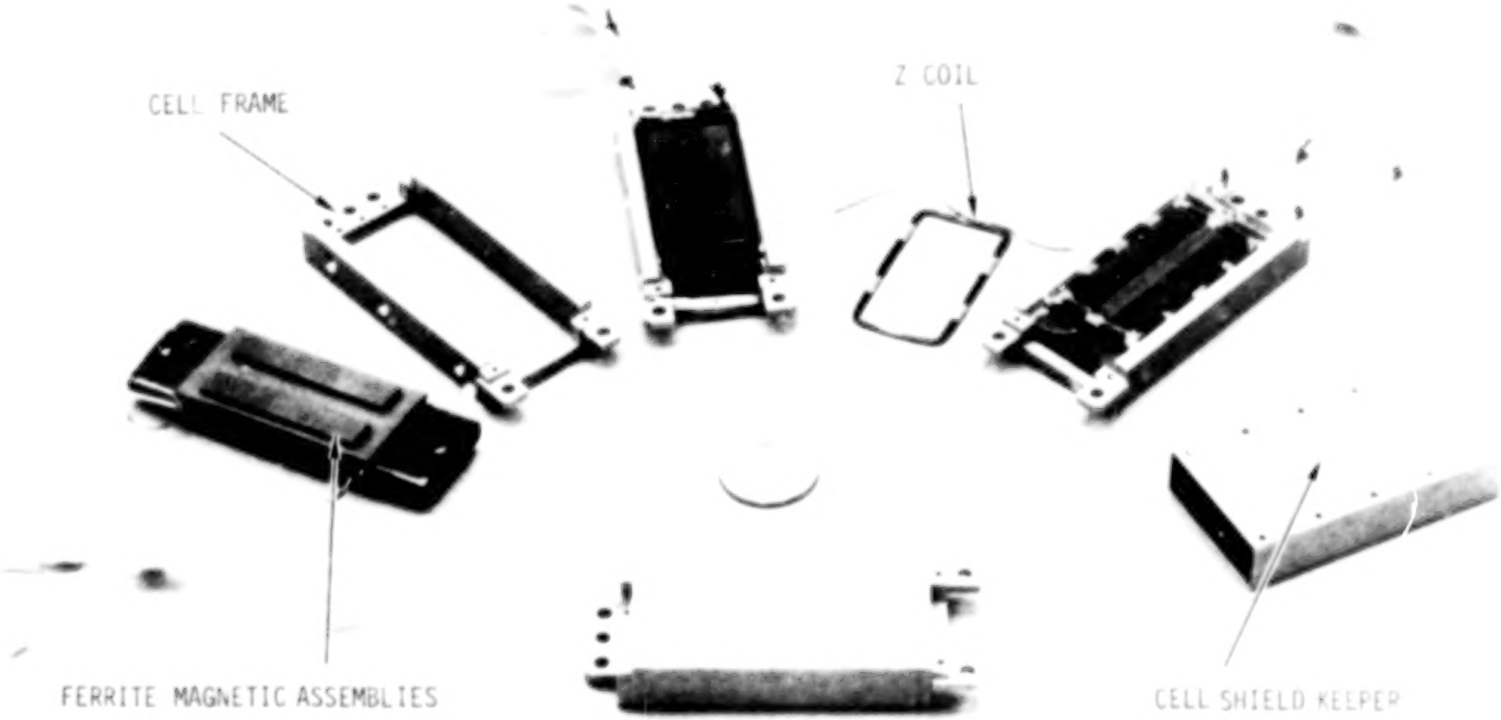
CELL FRAME
Z COIL
FERRITE MAGNETIC ASSEMBLIES
CELL SHIELD KEEPER

Fig 4-14. Cell Magnetics Details

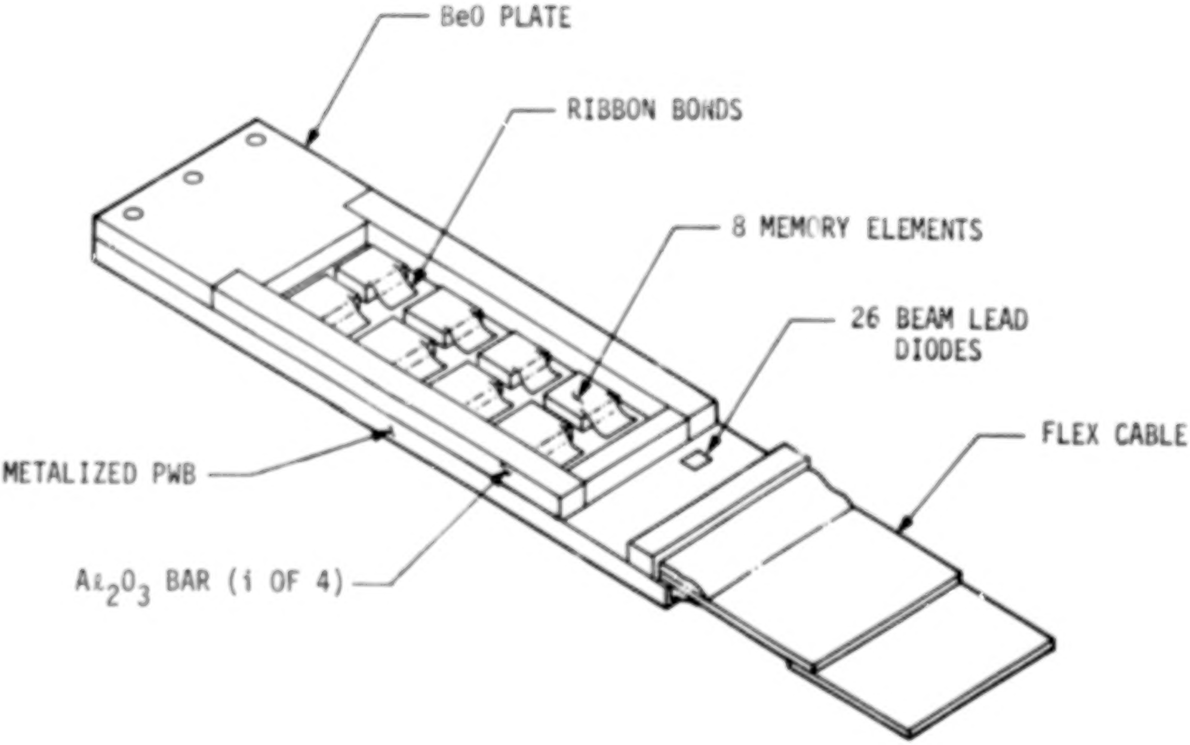
BeO PLATE
RIBBON BONDS
8 MEMORY ELEMENTS
26 BEAM LEAD DIODES
FLEX CABLE
METALIZED PWB
Al_2O_3 BAR (1 OF 4)

FIGURE 4-15. CARRIER

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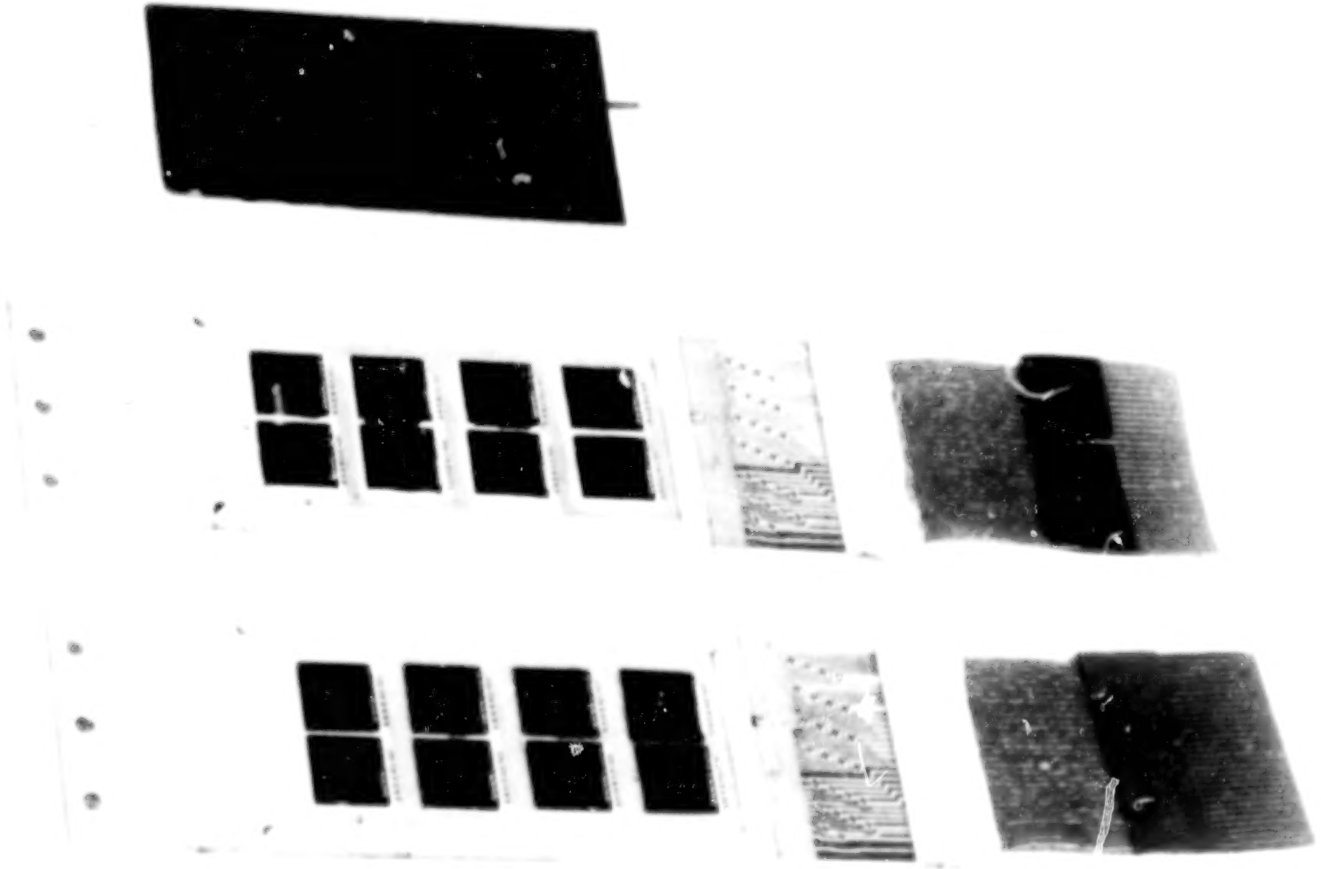


Fig 4-16. Cell Carrier Components

It is necessary to precisely control the geometry of the detector ribbon interconnect in order to minimize injection of noise produced by imbalanced dϕ/dt input from the rotating field. Uniform geometry bonds as shown in Figures 4-17(a) and 4-17(b) are produced by a modified ribbon feeding ultrasonic bonder.

Bubble chip operator functions are interconnected using 1 mil diameter gold wires which are terminated using a pulse thermocompression bonding process. This material and process were found necessary in order to assure acceptable bond strength at the aluminum-copper alloy operator function termination pads. Metallization properties of these pads were found to be not compatible with ultrasonic bonding.

A silicone elastomer insulated flexible cable having thirty stranded wire conductors on 25 mil centers is solder terminated to the carrier and strain relieved using an epoxy adhesive. This cable provides interconnection test to the memory module at final assembly.

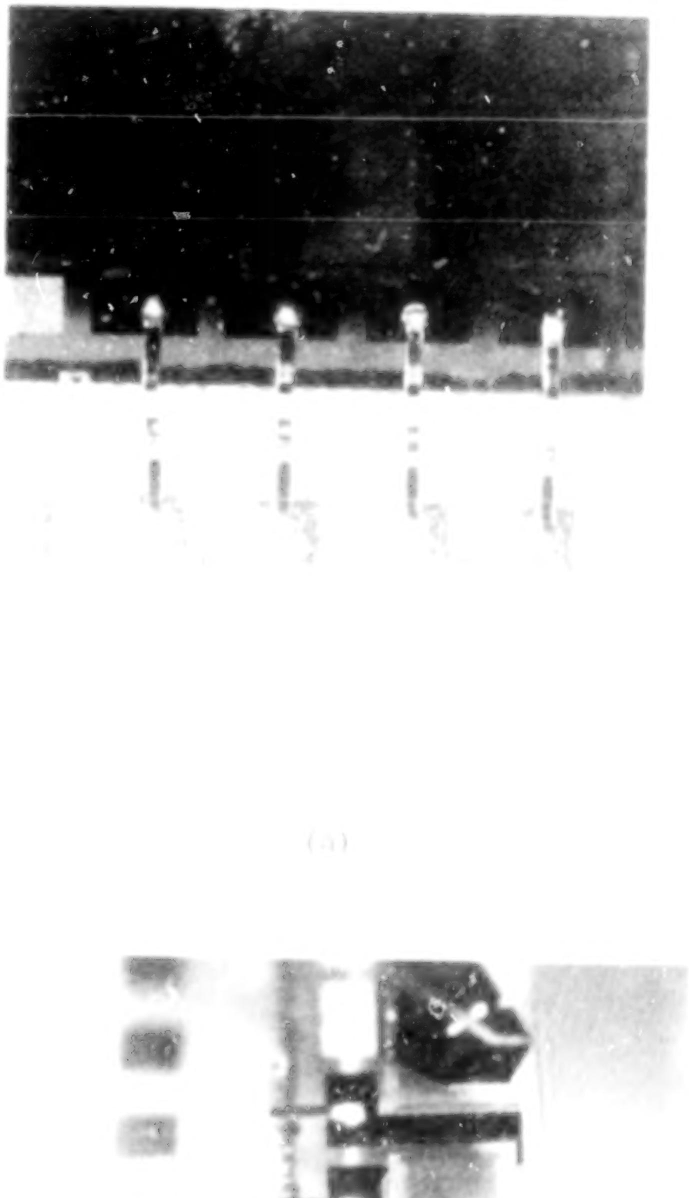
The dual carrier, illustrated in Figure 4-18, is an assembly of two carriers, indium plated copper shims and an insulated copper cover. The dual carrier has a storage capacity of 1.6×10^6 bits, is .127 in. thick, .860 in. wide and 3.020 in. long.

Two identical carriers, as previously described, are aligned, stacked and separated by indium plated chem milled copper shims. The two carriers are adhesively bonded together using an elastomeric urethane resin applied along the lateral interface between the two carriers. A 4 mil thick insulated copper cover is located as shown in Figure 4-18 and adhesively bonded to the top carrier. The cover is electrically grounded by soldering a tab to an adjacent exposed platinum gold pad on the PWB.

4.6.2 Magnetic Assembly

Principle components of the magnetic assembly as shown in Figure 4-19 include the X and Y coils, magnetic and ferrite assemblies, Z perturb coil, frame and permalloy shield keeper. X and Y rotating field coils (see Figure 4-19) produce the rotating field necessary for bubble propagation. The Y (outer) coil is wound as a free standing rectangular tube using two parallel connected layers of 5 mil by 25 mil heavy polyimide insulated rectancular magnet wire. A one mil polyimide film liner is adhesively bonded to the inner perimeter of the coil to provide additional insulation and mechanical integrity.

The X (inner) coil is designed such that a planar etched circuit configuration is folded into an open ended rectangular tube with lines (turns) oriented perpendicular to the open ends. This coil is magnetically equivalent to a wound coil which has turns which are parallel to the long axis but close off these ends which are open in the design implemented. The circuit laminate has 5 mil rolled and annealed copper adhesively bonded on two sides of a 2 mil



(a)

(b)

Fig 4-17. Detector Ribbon Interconnect

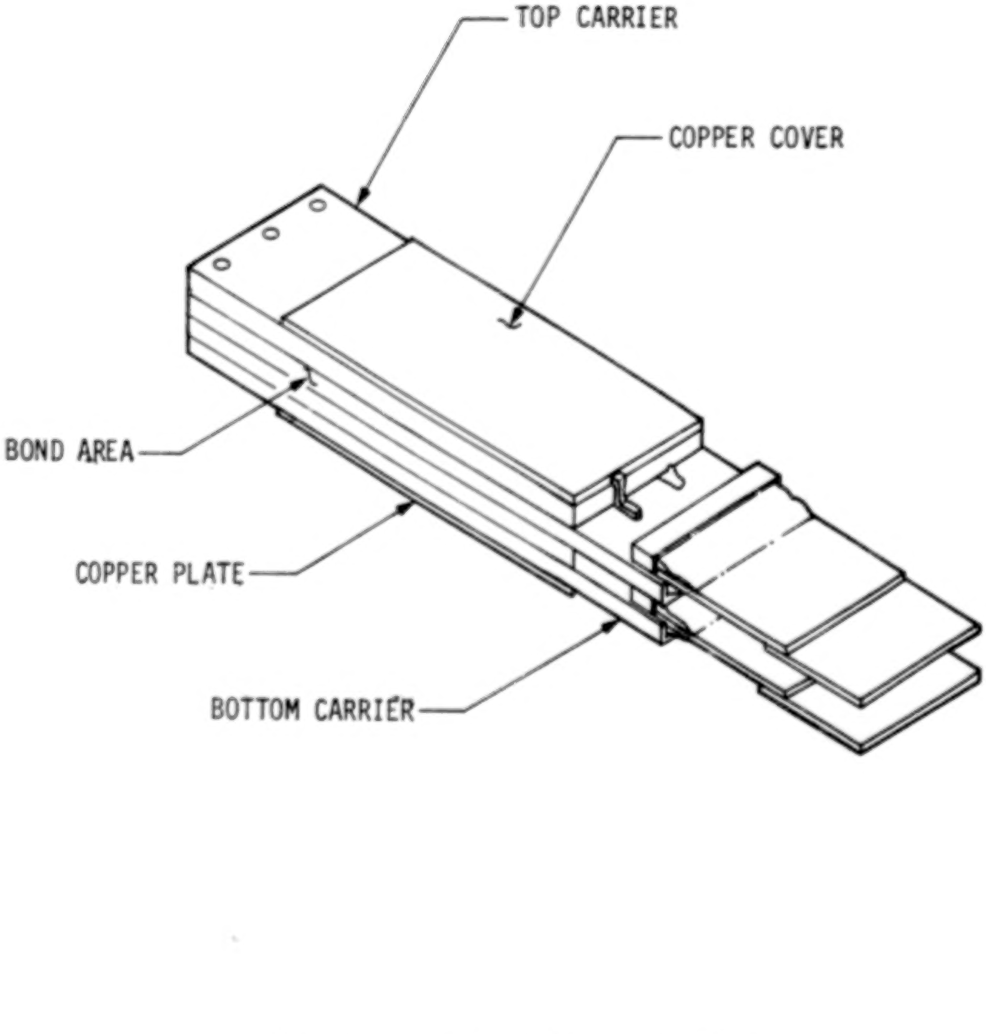

TOP CARRIER
COPPER COVER
BOND AREA
COPPER PLATE
BOTTOM CARRIER

FIGURE 4-18. DUAL CARRIER ASSEMBLY

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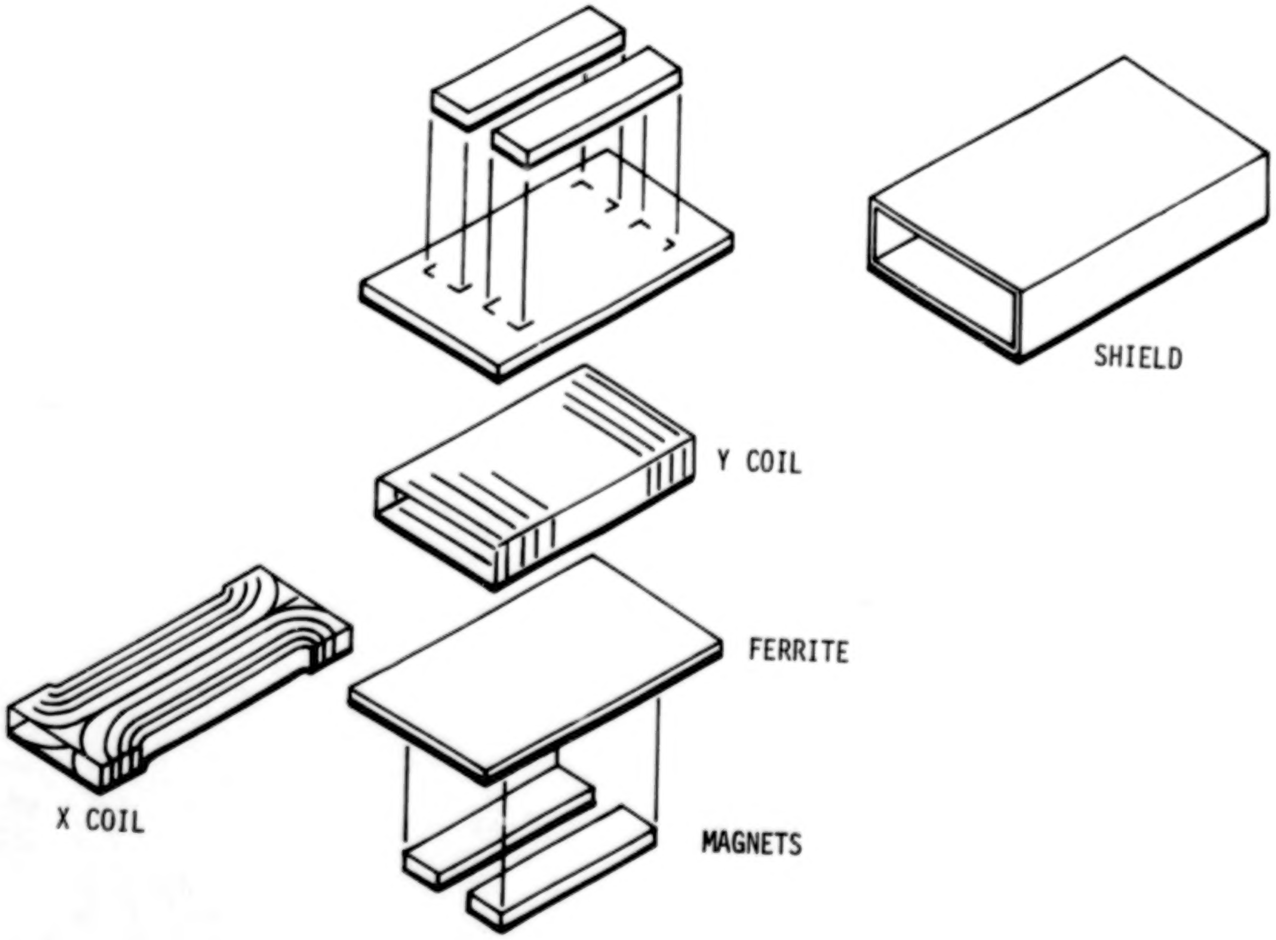
SHIELD
Y COIL
FERRITE
X COIL
MAGNETS

Fig 4-19. Cell Magnetic Assembly (Exploded)

polyimide film core and cover coated both sides after etching with adhesively bonded 1 mil polyimide film. Lead wires are soldered such that the two circuit sides are connected in parallel after which it is folded into the rectangular tube. The closing seam is electrically insulated and joined by a 1 mil polyimide film strip which is adhesively bonded in place.

The X and Y coils are adhesively bonded into an aligned assembly using a 3 mil high flow epoxy bonding film. This assembly is accomplished by collapsing and freezing the X (inner) coil (preform in place) and sliding it into the Y (outer) coil. A close fitting mandrel is inserted into the X (inner) coil causing it to expand and lock in place whereupon the coils and mandrel are clamped and the adhesive cured.

The four rare earth ceramic magnets and two ferrite field homogenizer-spreader plates are incorporated to produce a uniform Z axis magnetic field which is required to stabilize the bubble chip magnetic domains. These components are purchased in assembled form where each ferrite plate has two magnets located and adhesively bonded to one side. This assembly is finish ground flat and parallel to within .001 total. The individual assemblies are .093 in. thick, 1.05 in. wide and 2.15 in. long.

The two magnet and ferrite assemblies are bonded parallel to one another on opposite sides of the X-Y coil assembly. A Z perturb coil fabricated from 5 mil by 25 mil heavy polyimide insulated magnet wire is adhesively bonded to one of the magnet and ferrite assemblies as is shown in Figure 4-14.

The completed assembly is then aligned with and adhesively bonded in a frame which is milled from 6061-T6 alloy aluminum. This bonding is accomplished by injection of a high thermal conductivity alumina filled adhesive into holes penetrating two of the frame walls. The adhesive to frame interface and frame walls are the principle conduction paths for heat generated by the coils.

The shield keeper is an open ended rectangular tube fabricated from .03 in. thick permalloy (80-20 Ni-Fe alloy) which fits over the frame and is held in place by ten 0-80 flat head screws. Fabrication of the tube includes annealing for maximum permeability in order to meet shielding, attentuation and saturation requirements.

4.6.3 Cell Assembly

The dual carrier assembly, magnetic assembly and dual carrier mounting hardware comprise the components required for cell assembly. Preparation for assembly includes magnetizing the magnets in the magnetic assembly to a level which is determined by the composite bias margin of the 16 chips in the dual carrier designated.

Sizing and orientation of the X (inner) coil and frame are such that the dual carrier assembly is positioned in axial alignment within the X (inner) coil and tilted 2.3° with respect to the parallel ferrite plates which have been bonded to the X-Y coils. This tilt is required in order to provide a component of the Z magnetic field in the X direction and is established by inclined surfaces machined into the magnetic assembly frame.

Indium plated copper shims are located between the dual carrier assembly and inclined frame surfaces at both ends of the cell. One end of the dual carrier assembly is clamped and pinned in precise alignment to the frame and coils by an elastometer padded clamp bar assembly with integral press fit pin. This pin passes through the central hole (one of three) in the dual carrier assembly and frame. Two 0-80 socket head cap screws are threaded into the clamp bar from the frame and are torqued in place. The resultant force produced by the two screws is intended to cause the indium plating to conform to its various interfaces and produce a low thermal resistance.

The opposite end of the dual carrier assembly is aligned by the side walls of the inclined frame surface and is lightly clamped in place by an elastometer padded clamp bar which is secured by two 0-80 socket head cap screws. This clamp design is implemented to allow necessary slippage to length changes produced by differential expansion between the dual carrier and magnetic assemblies.

5.0 MEMORY MODULE DESIGN

5.1 INTRODUCTION

This section considers the detail design of the memory module configuration established in the preliminary design phase of the program. Section 5.2 describes the block level organization and function of the memory module and Section 5.3 the circuit implementation of the design.

5.2 MEMORY MODULE ORGANIZATION

The basis for the memory module organization was established in Sections 3.0 and 4.0 in terms of data storage subsystem partition and memory cell configuration. That design definition leads to a Data Storage Subsystem consisting of two memory modules. Each of the memory modules is functionally independent and contains thirty-two memory cells of sixteen memory elements each and the cell interface circuitry required to access these cells to read or write data. A general block diagram of the memory module is given in Figure 5-1. As noted in the figure, dual redundant A and B interfaces are provided as a fault tolerant feature. Table 5-1 summarizes the memory module interface for either A or B operation.

Using Figure 5-1 and Table 5-1, a block level functional description of the memory module design is given in the following paragraphs. In order to minimize standby power, voltages to the memory module are switched off by the power control section when the module is unused. The enable term applies power and puts the memory module in a condition to receive and execute commands. The enable term also determines which interface, A or B, controls the module. A module enabled with TEA will only respond to A signals. The power protect signal, PP, is a pulse which brackets the transition of the enable term and is used as an inhibit to prevent "glitches" from developing in the memory module circuitry during turn-on.

Three functions are selectable at the interface: write, erase and read. These are selected through the generate enable, annihilate enable and sense enable control terms. In addition to placing the memory module into a mode to perform the specified operation, these terms also serve to provide a second level of power switching by only providing power to the circuits associated with the selected operation. The five bit cell address, CS0-CS4, specifies the cell to be accessed.

As indicated previously, the memory module contains thirty-two memory cells. Coil drive for the memory cells is provided by two four by eight selection matrices: one for the X drive coils and one for the Y drive coils. The cell address provided at the memory module interface is decoded to result in coil drive being applied to the addressed cell. Timing for generating the actual coil drive current waveforms is provided by the X and Y timing terms, XCR, XT1-XT8 and YT1-YT8 which are supplied by the DCU.

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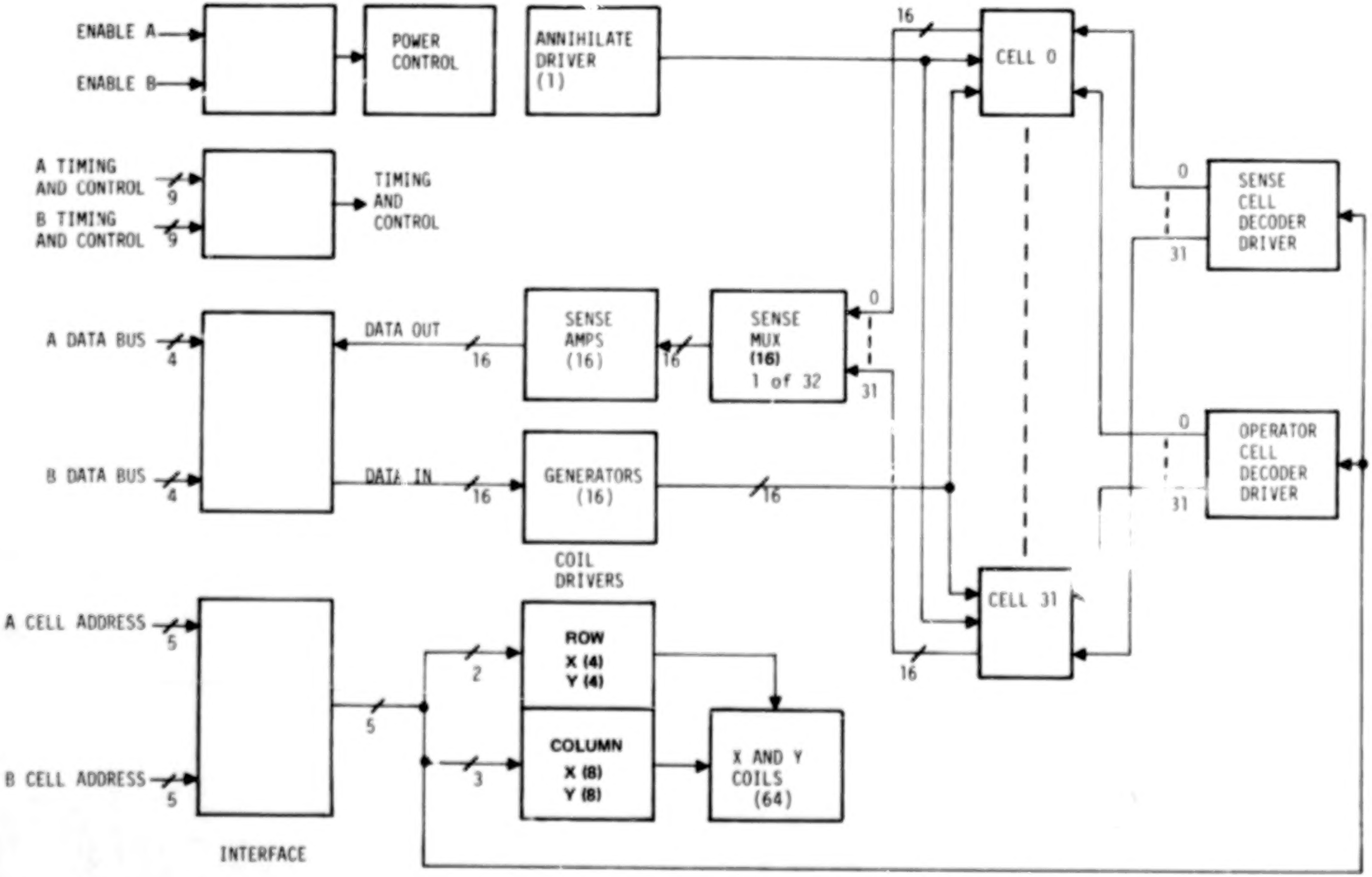
ENABLE A
ENABLE B
POWER CONTROL
ANNIHILATE DRIVER (1)
A TIMING AND CONTROL
9
B TIMING AND CONTROL
9
TIMING AND CONTROL
A DATA BUS
4
B DATA BUS
4
DATA OUT
16
SENSE AMPS (16)
16
SENSE MUX (16) 1 of 32
0
31
DATA IN
16
GENERATORS (16)
16
COIL DRIVERS
ROW X (4) Y (4)
COLUMN X (8) Y (8)
X AND Y COILS (64)
2
3
5
A CELL ADDRESS
5
B CELL ADDRESS
5
INTERFACE
16
CELL 0
CELL 31
16
0
31
SENSE CELL DECODER DRIVER
0
31
OPERATOR CELL DECODER DRIVER

Figure 5-1. Memory Module Block Diagram

Table 5-1. Memory Module Interface List

Term	Function	Type
PP	Power Protect	Power Control
TE	Track Enable	Power Control
CS0-CS4	Cell Address	Control
GE	Generate Enable	Control
AE	Annihilate Enable	Control
SE	Sense Enable	Control
AS	Annihilate Strobe	Timing
GS	Generate Strobe	Timing
SS	Sense Strobe	Timing
BS	Bridge Strobe	Timing
RS	Restore Strobe	Timing
DC	Data Clock	Timing
XCR	Coil Precharge Timing	Timing
XT1-XT8	X Coil Timing	Timing
YT1-YT8	Y Coil Timing	Timing
DB0-DB3	Data I/O	Data

Example: TEA = Track Enable on A Interface

Sensing is implemented by sixteen sense amplifiers which are multiplexed over the thirty-two cells through a linear selection matrix. A sense select switch is provided for each cell and when activated will result in connecting the sixteen chips in that cell to the sixteen sense amps. The sense select switch to be activated is determined by the cell address input in conjunction with the sense enable control term. Once the sense mode has been selected, coil drive timing is supplied to generate a rotating field cycle in the addressed cell. During this cycle, timing associated with sensing is supplied through the SS, BS and RS terms. Sixteen bits of data will be generated for every field cycle (150 KHz field rate). This data is converted to a four bit wide data stream at 600K bytes/sec. The DCU clocks the bytes out of the memory module onto the four bit wide bidirectional data bus with the data clock DC.

To write information into the module, a generate enable is supplied along with the address of the cell that is to be written into. The sixteen generator drivers are multiplexed over thirty-two cells by a linear select matrix. An operator select switch, when activated by the cell address, will connect the sixteen generator drivers to the sixteen chips of the addressed cell. Four four-bit bytes are then clocked into the memory module for every rotating field cycle by the DCU using the data clock. These sixteen bits are then written into the sixteen chips of the cell in parallel by the generate strobe timing pulse.

Because all chips are erased in parallel, the erase circuitry consists of a single annihilate driver which is multiplexed over the thirty-two cells by the same operator select switch that is used for a write operation. An erase operation is accomplished by applying the cell address, an annihilate enable control term, coil drive timing and an annihilate strobe timing pulse at the proper location in each cycle. Sixteen bits of data are then erased from the cell for each rotating field cycle.

A final possible mode of operation for the memory module is an align operation which moves the record within a particular cell without altering the content. This operation may be implemented by simply supplying the address of the cell to be aligned, along with coil drive timing. The record within the cell is moved sixteen bits for every rotating field cycle.

5.3 MEMORY MODULE DETAIL DESIGN

Fundamentally basic elements of the memory module design are the circuitry required to drive the memory element operator functions (generate and annihilate), sense circuitry and coil drive circuitry. A primary consideration in developing approaches to perform these functions was minimization of the parts count, thereby reducing system weight and volume. As indicated in the preliminary design discussion of Section 3.0, weight and volume were identified as critical items in attempting to meet design goals. Because of the importance of these functions to overall system characteristics, the considerations, rationale and resulting designs are discussed in detail in the following sections.

5.3.1 Operator Circuits

The purpose of the operator circuits is to provide generate and annihilate current pulses to the memory elements to perform erase and write functions. The annihilate pulse requires an amplitude of 110 ma ± 10% and a pulse width of 400 ns ± 5%. Generation requires a pulse of 150 ma ± 10% which is 140 ns ± 5% wide. Since there are 512 memory elements in a fully populated memory module, it is clearly impractical to provide a driver for each chip. The alternative is to provide sufficient drivers to operate a single cell and multiplex them over the cells in the memory module. This would then require sixteen drivers along with the necessary matrixing circuitry to provide the memory module generate function. Since all chips in a cell are erased simultaneously, in principle only a single annihilate driver in a matrix configuration would be required if the annihilator loops of all chips in the cell are connected in series. However, back voltage limitations will allow only four chips to be driven in series. Because of this, a minimum of four annihilate drivers with associated matrix circuitry are required.

Based on this concept, an operator matrix consisting of sixteen one-of-thirty two linear select channels for generate and four one-of-thirty two linear select channels for annihilate was designed. The same cell select switches are used for the annihilate and generate drivers. Figure 5-2 illustrates the general matrix configuration for a channel of the generate and annihilate function. When the select switch is off, the select bus on the unselected cells is held at -5 volts, back biasing the matrix diodes and decoupling the cell from the generate and annihilate drive lines. With the select switch on, the select bus is at +5 volts, forward biasing the matrix diodes and providing a path for the drive current. The circuit configuration for the select switch is as shown in Figure 5-3. Since the cell select switch must be capable of sourcing a total of 3.2 amps if all the generators in the cell are driven, the select switch utilizes four drive transistors with each transistor selecting four chips in the cell.

The operator current source design is illustrated in Figure 5-4. This design is such that standby power is essentially zero and the current source may be directly driven by low power TTL. Current amplitude is determined by a clamp reference voltage and the emitter resistor of the output transistor. Generator and annihilator drivers are identical except for the value of the emitter resistors.

The actual matrix is organized such that there are only sixteen select switches with each switch selecting two cells. Generator and annihilator drivers are duplicated with each group matrixed over half of the cells in the memory module. Selection of a specific cell is then made by a combination of a two-of-thirty two cell select switch and a one-of-two device selection. Since the driver and select switch have similar parts counts, this approach has no significant impact on total parts count but does eliminate a single point failure

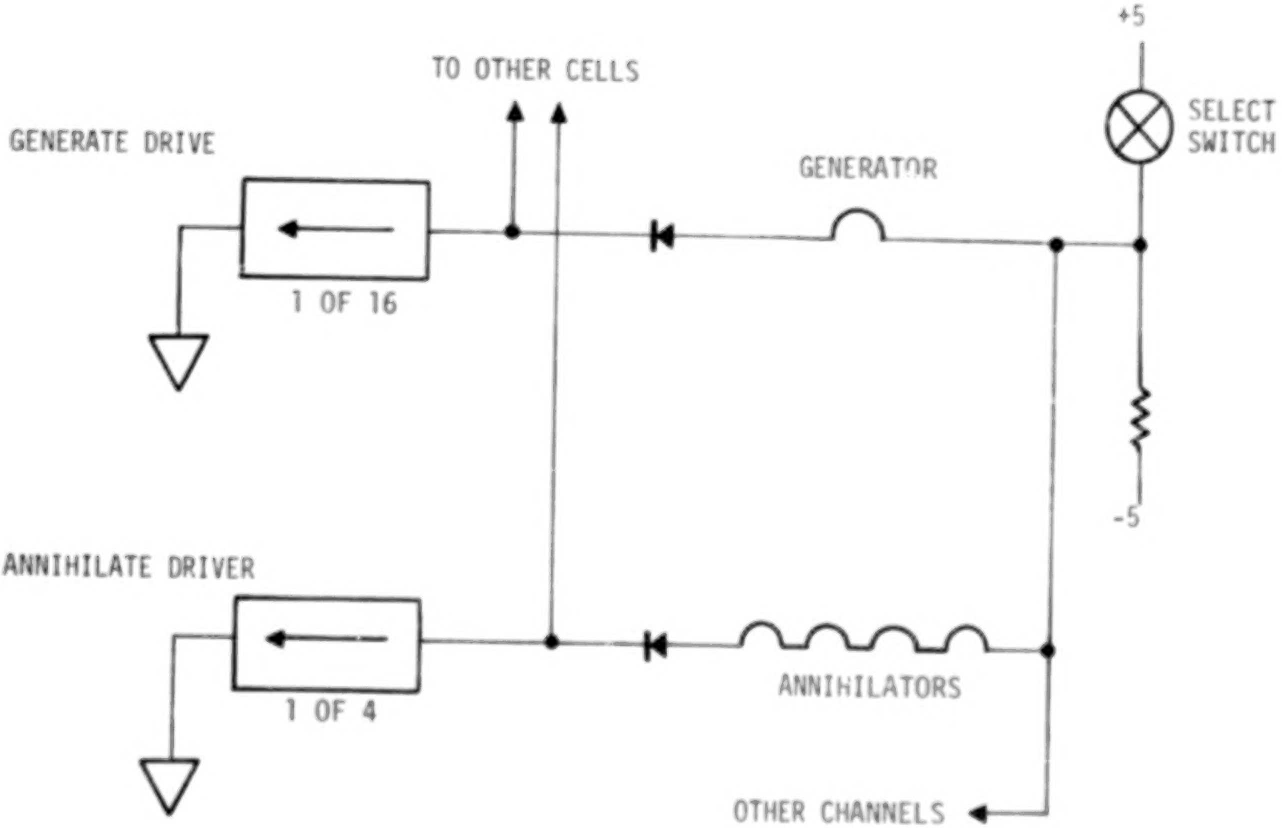
+5
TO OTHER CELLS
SELECT SWITCH
GENERATE DRIVE
GENERATOR
1 OF 16
-5
ANNIHILATE DRIVER
ANNIHILATORS
1 OF 4
OTHER CHANNELS

Figure 5-2. Annihilate and Generate Channel

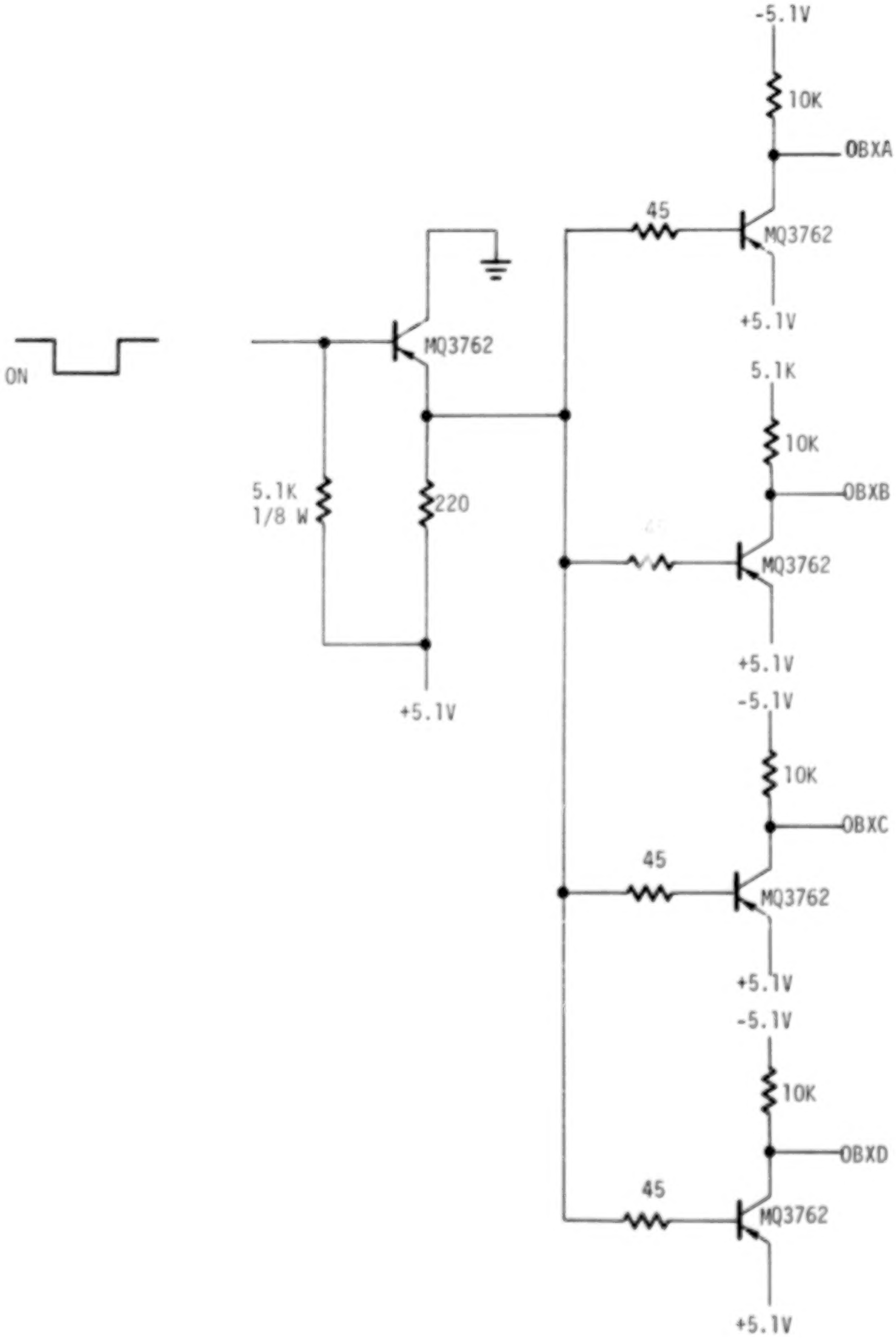
-5.1V
10K
OBXA
45
MQ3762
+5.1V
ON
MQ3762
5.1K
10K
OBXB
5.1K
1/8 W
220
45
MQ3762
+5.1V
+5.1V
-5.1V
10K
OBXC
45
MQ3762
+5.1V
-5.1V
10K
OBXD
45
MQ3762
+5.1V

Figure 5-3. Operator Bus Select Switch

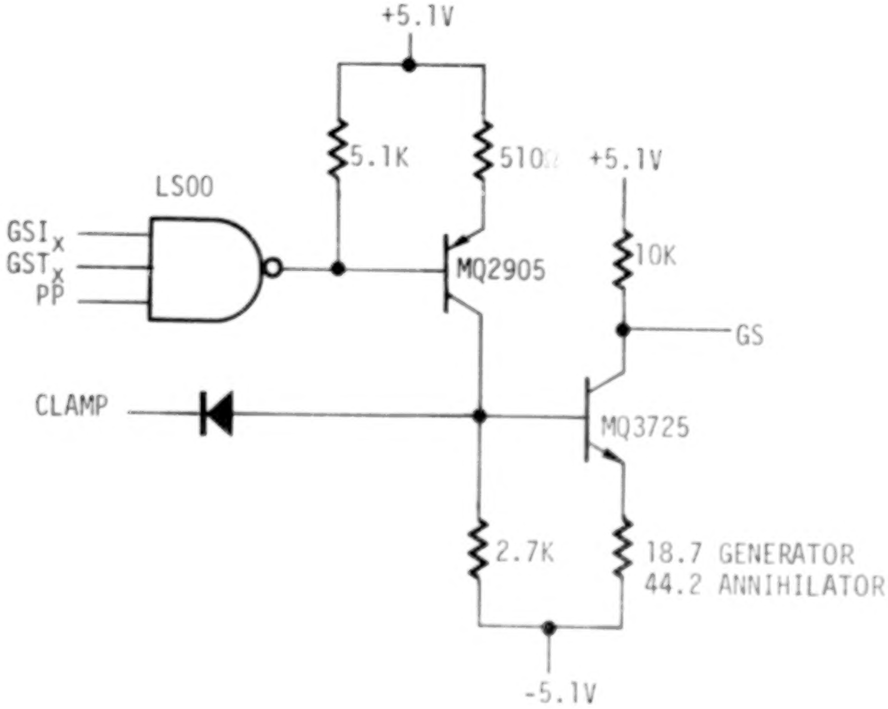
+5.1V
5.1K
510Ω
+5.1V
LS00
GSI$_X$
GST$_X$
PP
MQ2905
10K
GS
CLAMP
MQ3725
2.7K
18.7 GENERATOR
44.2 ANNIHILATOR
-5.1V

Figure 5-4. Operator Current Source

possibility. With two groups of drivers, a driver failure will eliminate only half the memory capability rather than all as would be the case with a single group of drivers.

5.3.2 Coil Drive Circuit

Considerable effort was expended in developing an approach to driving the memory cell coils. Techniques considered included resonant drive and voltage switched drive using a triangular or trapezoidal current waveform. A resonant drive approach results in the lowest power consumption since the losses in a parallel tuned tank circuit are only intrinsic coil and capacitor losses. For a voltage switched drive, the coil current not only flows through the drive coils, but also through the series drive elements used to control the current which results in additional power dissipation. However, resonant coil drive has a number of disadvantages which tend to offset the lower power. First, the power advantage of a resonant drive may be realized only if the driver is run for many cycles each start-stop sequence. This is due to the fact that stopping a resonant drive requires dissipation of all coil drive energy while stopping a voltage switched drive results in partial return of energy to the voltage source. Thus, for short burst mode operation, a switched coil drive may actually have lower power dissipation. It should also be noted that the stop operation for a resonant drive will require one or more cycles, limiting data rate in a burst mode of operation. Resonant coil drive does not adapt to a matrixed drive configuration, resulting in a large parts count which is further compounded by the large physical size of the tuning capacitors required. Also, each individual coil would require capacitor trimming to obtain the proper resonant frequency, making each cell position unique and preventing direct cell interchangeability. The phase stability of a resonant circuit over all operating conditions also is a potential problem. Because of these problems, it was determined that a voltage switched coil drive was the most feasible approach for the SSDR with parts count being a primary consideration.

Once a voltage switched coil drive approach was selected, it was necessary to choose between a triangular and trapezoidal current waveform. Circuitry required for either approach is identical except for timing. At the time this design was being finalized, insufficient data was available to relate triangle drive amplitude requirements to the available sine drive memory element characterization data. Because of this, a trapezoid drive approach was selected because it closely approximates sine drive characteristics.

The basic coil drive system is illustrated in Figure 5-5. Initially, switches A and D are turned on allowing the coil current to increase at a rate determined by the L/R time constant of the coil. When the peak amplitude is achieved, the A switch is turned off - allowing current to circulate through a low impedance path formed by D_A and switch D. The current is then reduced to zero by turning off switch D and discharging the coil into the +V supply through a path provided by D_A and D_C. The negative half of the drive cycle is generated by a similar process using switch B and switch C. The insert in Figure 5-5 illustrates the rotating field locus generated with this type drive compared to the circular locus generated by an ideal sine drive. It may be seen from this that this coil drive technique closely approximates the field that would be generated by sine drive.

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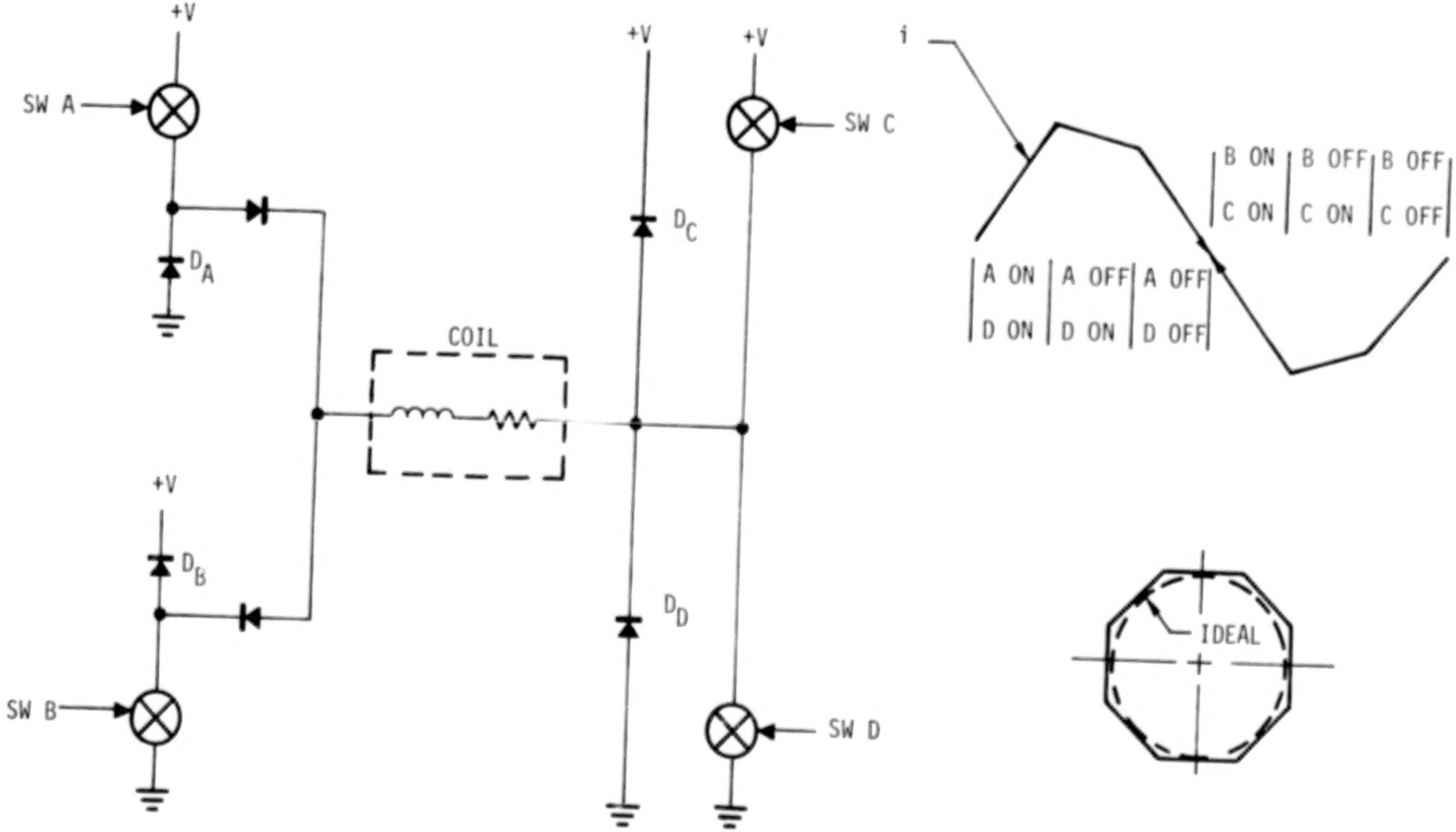

+V
SW A
D_A
+V
D_B
SW B
COIL
+V
D_C
D_D
+V
SW C
SW D
i
A ON
D ON
A OFF
D ON
A OFF
D OFF
B ON
C ON
B OFF
C ON
B OFF
C OFF
IDEAL

Figure 5-5. Coil Drive Configuration

The coil drive approach was to adapt the basic coil drive technique described above to matrixed configurations that would provide drive for the thirty-two cells on the memory module. In addition, the drive circuitry was required to provide a precharge drive waveform which was required for first bit read. When the bubble device is in an undriven state, bubbles in the detector track collapse to a normal bubble from the strip condition they exist in when driven. The bubble must be stripped out to the full width of the detector track for proper detection. Because of this, the X field must be increased to its full amplitude and held for a period prior to starting rotation. This allows time for the bubble to strip out prior to making it into the detector. The coil driver was designed to provide up to three cycles of precharge.

The final coil drive design arranged the cells in a 4 x 8 matrix. With the exception of the precharge circuitry, both the X and Y row and column drivers were designed identically. Also, the row switches were exactly the same as the column switches in design. Only the timing signals were different. A block diagram of the cell and matrix switches is shown in Figure 5-6. The matrix switch detail is shown in Figure 5-7 and the precharge schematic in Figure 5-8. The coil interconnection is shown in Figure 5-9.

The precharge circuit of Figure 5-8 operates in the following manner. The logic term XCR is normally low when coil driver is not operating. Also, +5 VH is a power strobed +5 volt supply which is low when the track is not selected. This prevents the power switch from turning on prior to track selection. Capacitor, C2, is charged through R6 for the initial precharge if the first operation is a read cycle. When the track is enabled XCR is controlled to the low state, +5 VH is power strobed on and subsequently the selected operating mode determines if XCR is made high. For all operating modes except read, XCR is made high prior to activation of the coil driver switches. In the read mode, XCR is held low during the precharge period. The peak coil current is supplied by C2 and the steady state current is established by the +15 volt supply and the parallel resistor R1 and R2. At end of precharge, XCR is made high-turning on the power switch. This reverse biases CR2-disconnecting the precharge resistors.

The matrix driver switches are all identical and are shown in Figure 5-7. A center-tapped transformer is used to drive the switch transistor off as well as on to minimize turnoff time and associated switching power loss. The switch transistors are operated in an unsaturated mode to further reduce turnoff time. Clamping diodes CR1 through CR4 insure that the inductive voltage spikes do not exceed the 55462 predriver output specification. The resistors R3 and R4 were added to stabilize the matrix lines to a known potential to prevent sneak current paths for the unselected coils. Also, ultra fast recovery diodes were selected for CR5 and CR6. This was required to minimize the current undershoot occurring in the last (stop) cycle.

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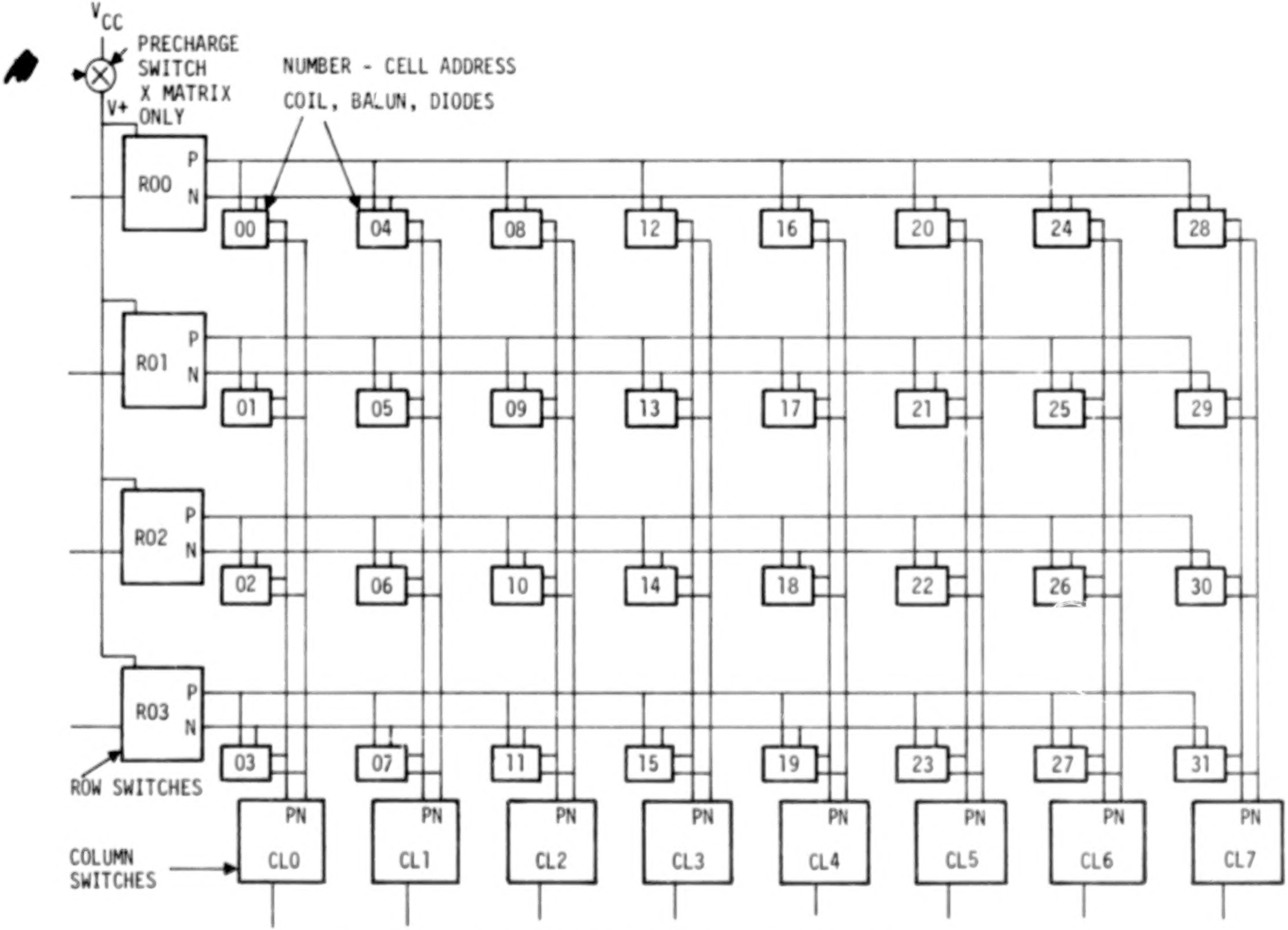

V_CC
PRECHARGE SWITCH X MATRIX ONLY
V+
NUMBER - CELL ADDRESS
COIL, BALUN, DIODES
R00
R01
R02
R03
P
N
00
01
02
03
04
05
06
07
08
09
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
ROW SWITCHES
COLUMN SWITCHES
PN
CL0
CL1
CL2
CL3
CL4
CL5
CL6
CL7

Figure 5-6. Coil Matrix Block Diagram (one of two)

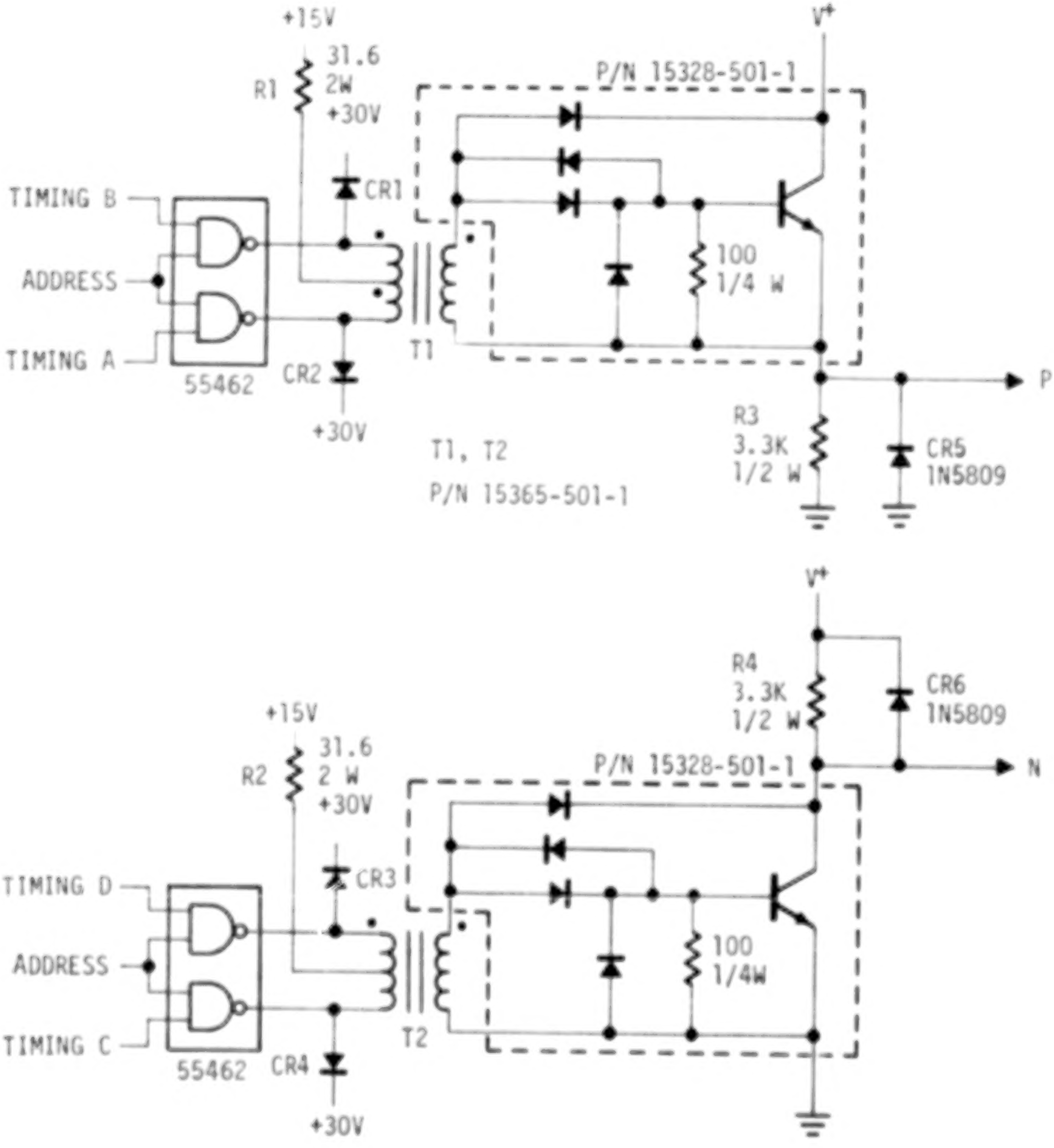

+15V
R1
31.6
2W
+30V
V+
P/N 15328-501-1
TIMING B
ADDRESS
TIMING A
CR1
CR2
55462
+30V
T1
100
1/4 W
T1, T2
P/N 15365-501-1
R3
3.3K
1/2 W
CR5
1N5809
P
V+
R4
3.3K
1/2 W
CR6
1N5809
N
+15V
R2
31.6
2 W
+30V
P/N 15328-501-1
TIMING D
ADDRESS
TIMING C
CR3
CR4
55462
+30V
T2
100
1/4W

Figure 5-7. Matrix Driver Switch (One of Twenty-four)

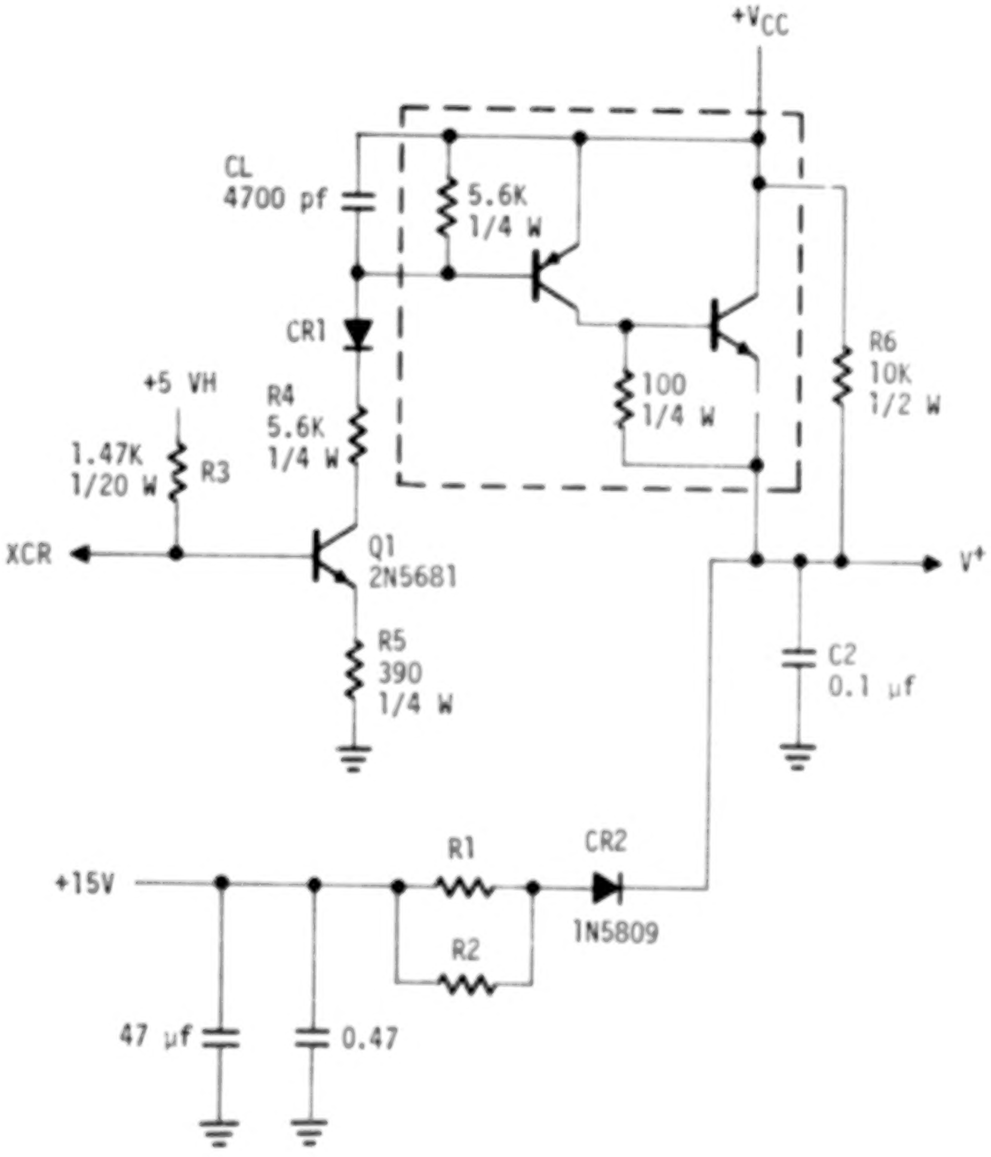

+V_CC
CL
4700 pf
5.6K
1/4 W
CR1
100
1/4 W
R6
10K
1/2 W
+5 VH
R4
5.6K
1/4 W
1.47K
1/20 W
R3
XCR
Q1
2N5681
V+
R5
390
1/4 W
C2
0.1 μf
R1
CR2
+15V
1N5809
R2
47 μf
0.47

Figure 5-8. Precharge Switch

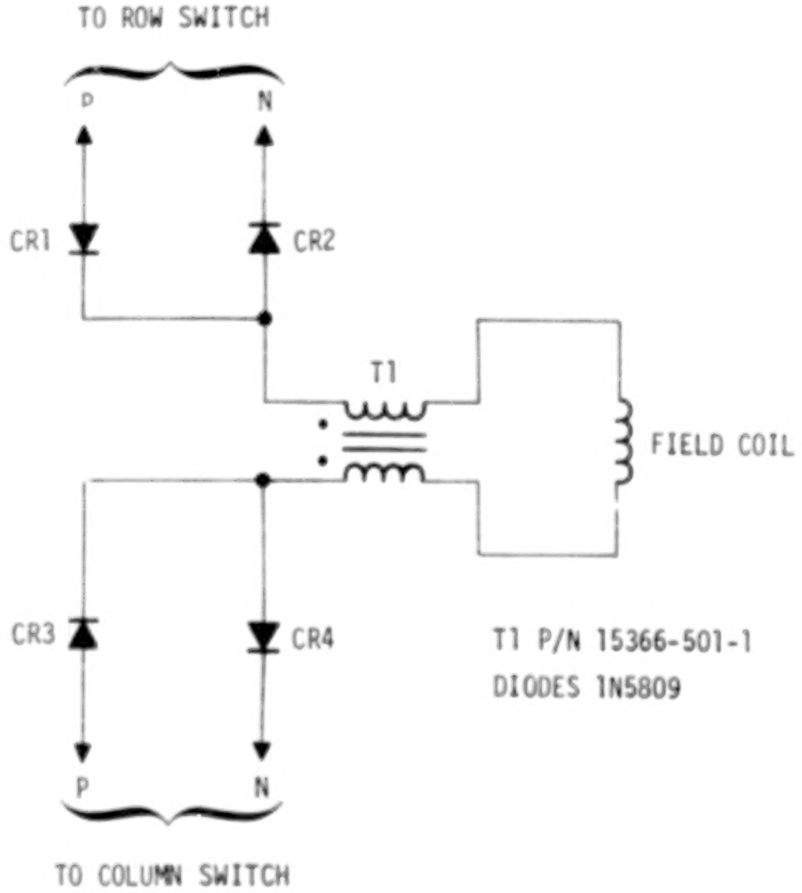

TO ROW SWITCH
P
N
CR1
CR2
T1
FIELD COIL
CR3
CR4
T1 P/N 15366-501-1
DIODES 1N5809
P
N
TO COLUMN SWITCH

Figure 5-9. Coil Interconnection Detail (1 of 64)

During breadboard testing of a 2 x 2 matrix, it was found that additional isolation was required for satisfactory performance of the coils in a matrix. The form of this isolation is illustrated in Figure 5-9 and consists of four diodes and a balun transformer. The primary purpose of these components is to provide isolation of the unselected coils. As a secondary benefit, the balun provides isolation between X and Y coils, reducing circulating currents between coils associated with interwinding capacity. This problem is illustrated in Figures 5-11 and 5-12 which show the current flowing in an unselected X and Y coil in a matrix configuration. The top and bottom traces represent current flowing into the two leads of the coil. With the balun added, these currents in the unselected coils are reduced as shown in Figures 5-13 and 5-14. The balun also effects the current waveform of the driven coil. Without a balun, oscillation associated with the coil inductance and interwinding capacitance is clearly apparent in Figure 5-15. When isolation between X and Y coils is achieved by use of a balun, a considerably cleaner drive waveform, as seen in Figure 5-16, is obtained.

As discussed in Section 4.0, when device tolerance and cell field uniformity are taken into account, a total available drive field tolerance of 15% remains. This available tolerance must cover drive field variations caused by coil drive voltage variations, circuit component variations, cell sensitivity variations, and coil drive timing variations. The power supply was specified to provide a coil drive voltage with a 3% tolerance leaving 12% for circuit and cell sensitivity variations. Coil drive field sensitivity was specified at a total maximum allowable variation of 5% leaving 7% for component and timing variations under worst case conditions. The most significant factor to be taken into account by this remaining tolerance is the turn off storage time of the coil drive switches. To minimize this variation, a storage time specification was applied to the coil drive switch transistors and, as discussed previously, the switches were driven off with a low impedance source and were operated in a unsaturated mode.

After establishing the basic coil drive configuration and undertaking preliminary packaging, it was found that the high voltage and current requirements (60 volts, 3 amps) of the coil drive switches were only available in large (TO-5)case size. To minimize the required coil drive MLB surface area, it was decided to hybridize the coil drive switches. Each hybrid contained two of the basic switches as defined by circuitry within the dotted lines in Figure 5-7. Thus, each of the row and column switches of Figure 5-6 represent a hybrid.

The manner in which the timing terms XT1-XT8 and YT1-YT8 provided to the Memory Module by the DCU are used to generate this coil drive current is illustrated in Figure 5-10. This Figure shows one cycle of X

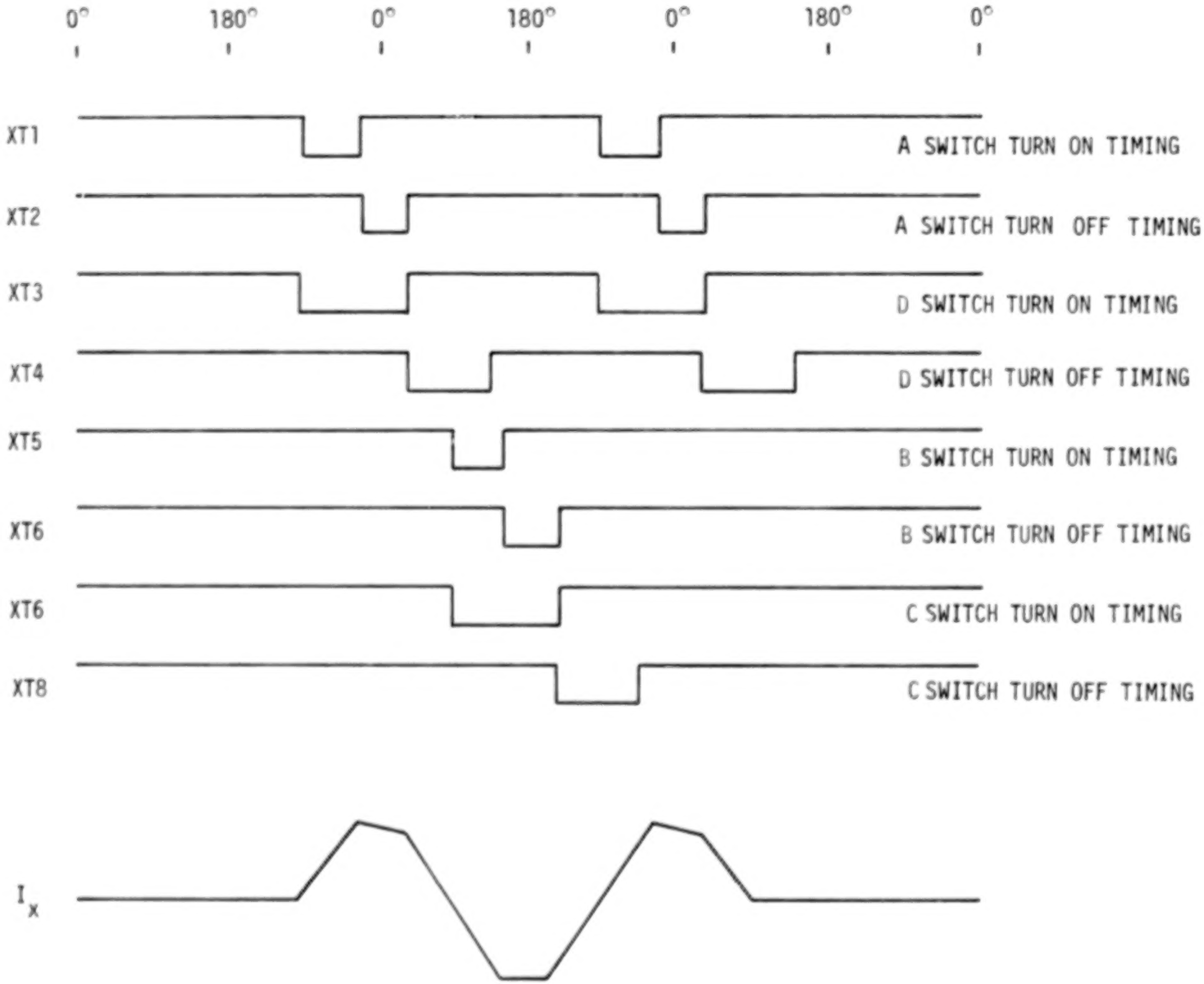
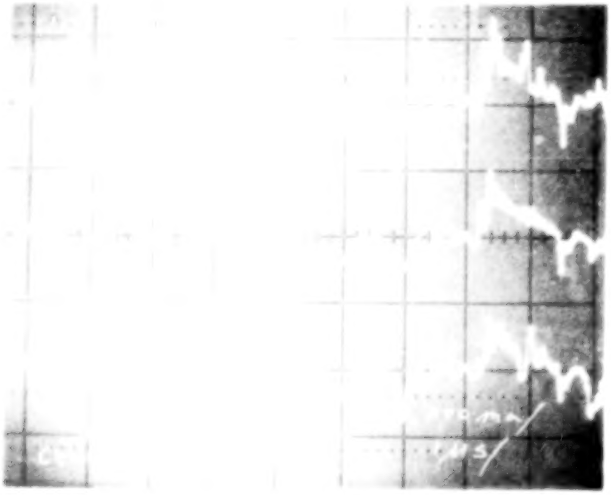

0°
180°
0°
180°
0°
180°
0°
XT1
A SWITCH TURN ON TIMING
XT2
A SWITCH TURN OFF TIMING
XT3
D SWITCH TURN ON TIMING
XT4
D SWITCH TURN OFF TIMING
XT5
B SWITCH TURN ON TIMING
XT6
B SWITCH TURN OFF TIMING
XT6
C SWITCH TURN ON TIMING
XT8
C SWITCH TURN OFF TIMING
I_x

Figure 5-10. Coil Drive Timing

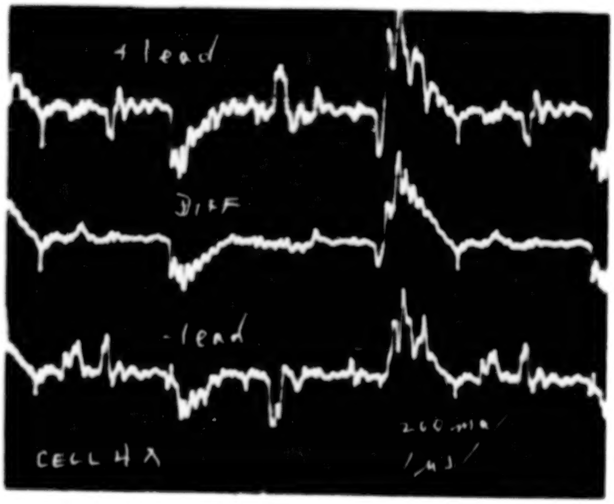


TOP - 200 mA/DIV

MIDDLE - 500 mA/DIV
CORRECTED

BOTTOM - 200 mA/DIV

Figure 5-11. Transient Current in the Unselected Y Coil without Balun

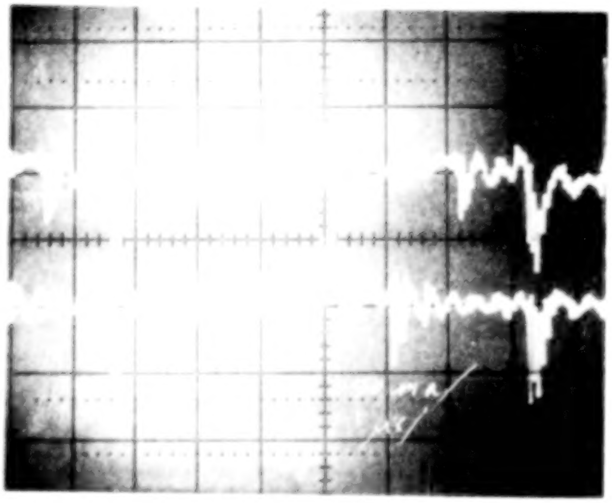


TOP - 200 mA/DIV

MIDDLE - 500 mA/DIV
CORRECTED

BOTTOM - 200 mA/DIV

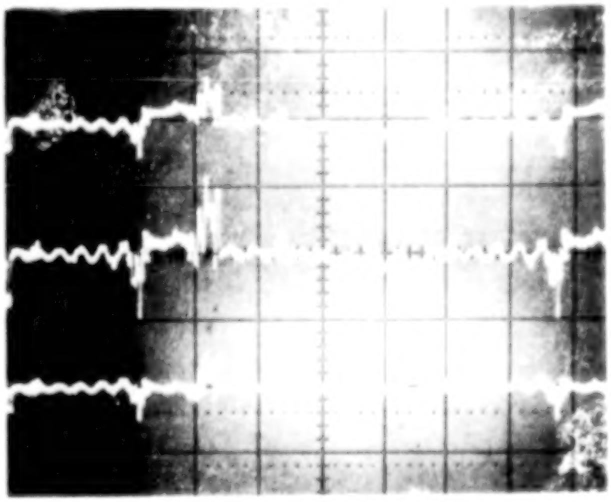
Figure 5-12. Transient Current in the Unselected X Coil without Balun



TOP - 50mA/DIV

BOTTOM - 50 mA/DIV

Figure 5-13. Transient Current in the Unselected Y Coil with Balun

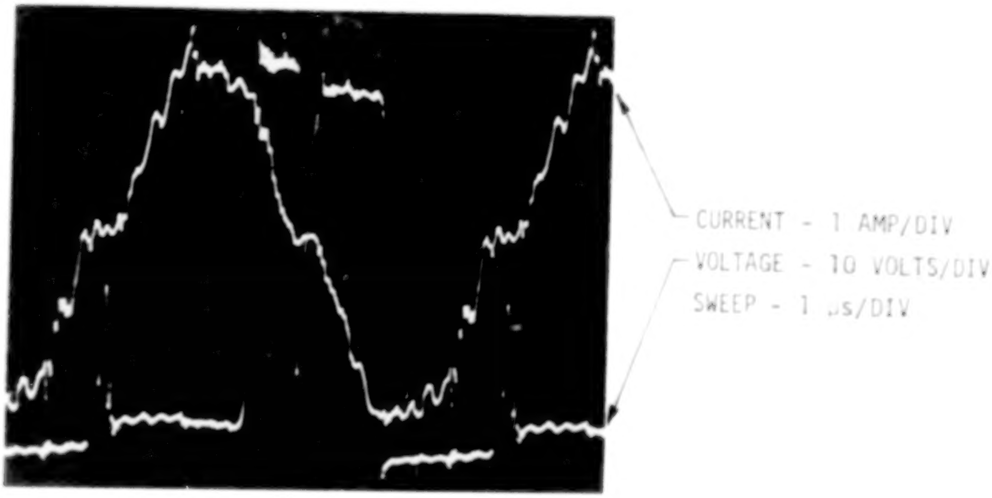


TOP - +LEAD 100 mA/DIV

MIDDLE - SUM +LEAD
AND -LEAD
200 mA/DIV
CORRECTED

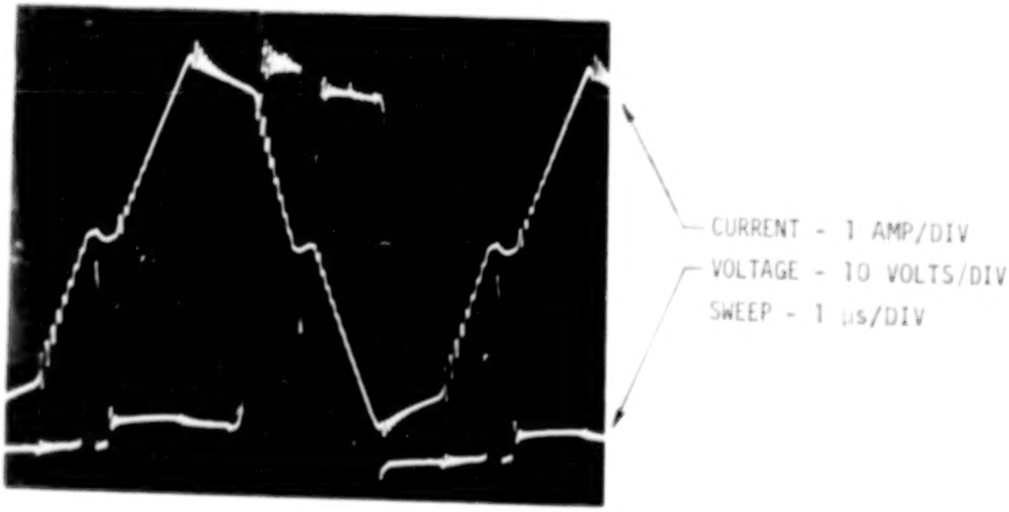
BOTTOM - -LEAD
100 mA/DIV

Figure 5-14. Transient Current in the Unselected X Coil with Balun



CURRENT - 1 AMP/DIV
VOLTAGE - 10 VOLTS/DIV
SWEEP - 1 μs/DIV

Figure 5-15. Coil Current without Balun



CURRENT - 1 AMP/DIV
VOLTAGE - 10 VOLTS/DIV
SWEEP - 1 μs/DIV

Figure 5-16. Coil Current with Balun

current with the corresponding timing terms. The A, B, C and D switch designations refer to Figure 5-5. Y current generation and timing is similar but displaced by 90°.

5.3.3 General Description of Sense Circuit

The sense electronics for each memory module consists of sixteen sense amplifiers and associated circuitry along with 32 sense bus selection drivers. The basic operation of a single sense channel may be described using the schematic of Figure 5-17. The S and D elements represent the active and dummy detector respectively of a chip in one cell. One side of each active and dummy detector are tied together and commoned with the same point on all other chips of the cell. This point is designated SBXX on the schematic and connects to the sense bus select driver SSWXX for that cell. The other end of the dummy and active detectors are connected to cathodes of beam lead diodes which are mounted on the memory cell substrate. The anodes of these diodes are tied to corresponding points on the other 32 cells and to the differential inputs of a sense channel. Thus all S0, D0 points on all cells are tied togehter and connected to a sense amplifier as are S1, D1, S2, D2, etc.

Operation and selection of the desired chips are done in a power switched mode to minimize power consumption. During read, one of the select switches, SSWXX, is energized which grounds all detectors in the selected cell. Subsequently, the power to the amplifier and the bridge current is turned on. Bridge current turn-on causes line capacitance and coupling capacitance to be charged, resulting in large current transients on the differential lines which are clamped or shorted to ground by the DC restore clamp transistors. When the line has settled, which takes typically 1 to 2 microseconds, the clamp transistors are turned off and the differential signal is sensed.

Functionally the channel includes a differential sense bus S(X)/D(X) which is connected to 32 memory element detectors, a current source pair to supply bridge current, an emitter follower to lower impedance, coupling capacitors, a clamp, and a latching sense amplifier.

These electronic design elements detect the bubble which manifests itself by a change in detector resistance. Signal level is only slightly larger than typical amplifier offsets while the system environment contains large transients, so that the choice of an AC coupled sense channel seems most logical. Initialization of the amplifier input to a differential zero is accomplished by first clamping the coupling capacitors to ground during turn-on transients and then releasing the clamp just before signal time. In

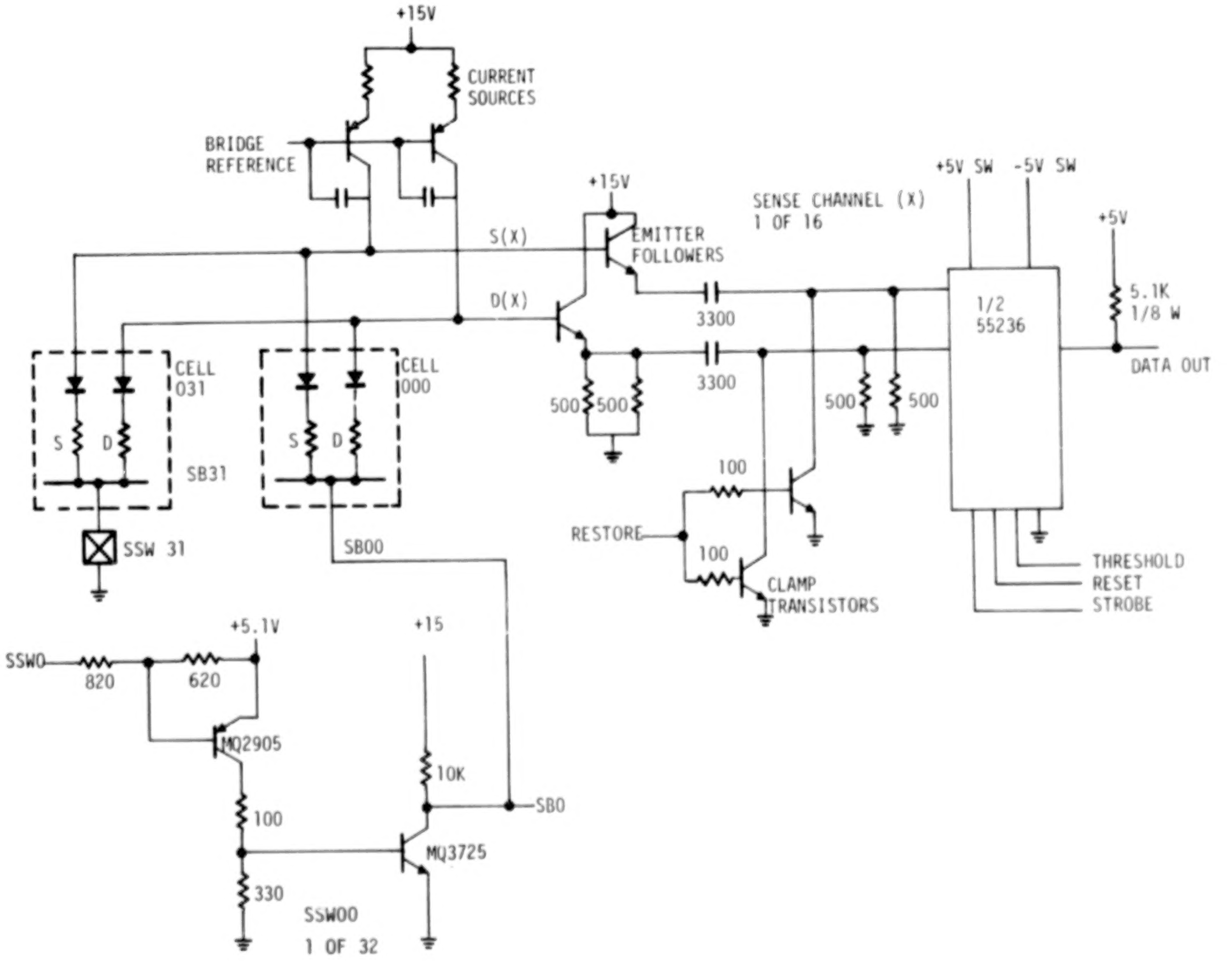

+15V
CURRENT SOURCES
BRIDGE REFERENCE
+15V
EMITTER FOLLOWERS
SENSE CHANNEL (X) 1 OF 16
+5V SW
-5V SW
+5V
S(X)
D(X)
3300
3300
1/2 55236
5.1K 1/8 W
DATA OUT
CELL 031
CELL 000
S
D
S
D
SB31
500
500
500
500
100
RESTORE
100
CLAMP TRANSISTORS
THRESHOLD
RESET
STROBE
SSW 31
SB00
+5.1V
+15
SSW0
820
620
MQ2905
10K
SB0
100
MQ3725
330
SSW00 1 OF 32

Figure 5-17. Sense Channel Schematic

order to minimize detector loading, high impedance current sources are used to provide the current for the detector and dummy, and emitter followers are used to increase the input impedance of the restore and aplifier circuitry.

Prior to committing to layout of the multilayer board for the memory module, a breadboard of the sense channel was built and tested. The channel contained all elements of the matrix including simulated loads and equivalents for unselected portions of the matrix. The channel was tested using both a simulated signal injected into the circuit and an actual signal which was obtained by connecting the differential pair to a 20 kilobit bubble test device.

Several tradeoffs were explored during this phase of development. First, the sense amplifier impedance, bias current requirement, and offset requirement establish an upper limit on equivalent signal source impedance of about 500 Ω. This in turn requires a coupling capacitor of 3300 pf to maintain a satisfactory bandpass for the bubble signal. The coupling capacitor consumes approximately 0.15 watt-μs of charging energy when the clamp transistor is on, which requires a low clamp impedance at relatively high current to charge the capacitor quickly. This is accomplished by using 2N2369 transistors in a saturated forward mode. The use of emitter followers ensures the equivalent generator impedance is sufficiently low. During turn-on of the bridge, surge currents on the order of 20-50 ma are experienced in each capacitor. This current has a settling time of approximately 500 nanoseconds. Another tradeoff involved the signal amplitude and the choice of amplifier. At the time of the evaluation, based on results from the 20 kilobit test chip, it appeared that signal could be increased significantly by increasing pulsed bridge current to a center value of 15 milliamps which would provide adequate detection (>10 mv) using a single low threshold (5-7 mv) 55236 sense amplifier rather than a preamplifier/amplifier combination. Based on this analysis, such an approach was adapted for use in MM design.

Overall, the breadboard performed satisfactorily from -10 C to 60 C and met the goals of low standby power and a reasonably low component count. All components of the channel with the exception of the 55236 militarized core sense amplifier were selected from space qualifiable parts lists. Derating was applied for power dissipation and breakdown voltages.

During the breadboard design, the decision was made to use a nonsinusoid trapezoid voltage switched coil drive. It was found that this would impact the sense channel noise because of the large high frequency voltage transients on the coil during the switching operation. These inflection points in the current and voltage waveforms of the trapezoidal wave drive cause considerable voltage to be injected into the sense channel because of the capacitance between coil and sense conductors on the coil substrate. A further complication is the fact that the two coils are capacitively coupled which causes some high frequency ringing on the drive waveform. A shield or guard between the coils and the sense lines was found beneficial in reducing this noise. Figure 5-18 shows the differential signal without shield and with a shield. The improvement in noise reduction with the Faraday shield is seen to be significant. This shield was implemented as part of the cell configuration.

5.3.4 Memory Module Status Sensing

Two monitoring functions are available to assess status and diagnose potential problems within the Memory Module. Coil drive power on the 60 volt bus is monitored and provided at a telemetry connector for each of the Memory Modules. (See Power Supply Section 7 for details.) In addition, temperature sensing of both Memory Modules is available. This sensing is provided by a thermistor which is mounted on a heat rail on the outboard side of the sense MLB. The temperature in degrees celsius is obtained from the resistance of the thermistor by the following expression;

$$T = 0.338 - 204 \ ^\circ\mathrm{C}$$

The thermistor resistance is about 600 Ω at 0°C. The thermistors for both Memory Modules are available at the telemetry connector.

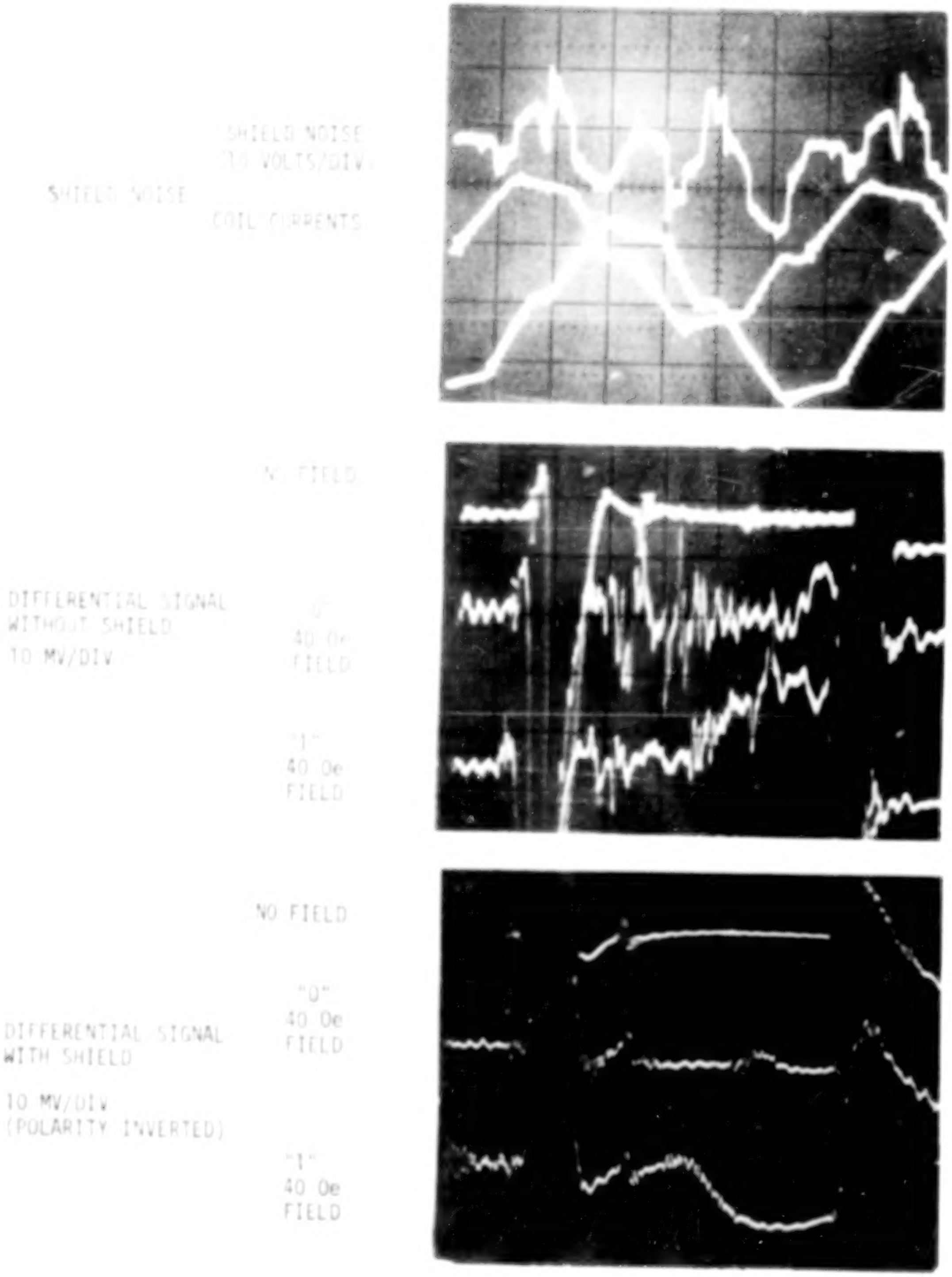


Figure 5-18. Trapezoidal Wave Noise

6.0 DETAIL DCU DESIGN

6.1 INTRODUCTION

As described in Section 3.0, the Drive and Control Unit (DCU) provides the user interface to the SSDR and buffers the flow of data between the System I/O and the MEMORY MODULES. This design provides the necessary control and data handling capability to allow the SSDR to operate as up to four independent serial data recorders or as a single channel eight bit parallel I/O recorder.

A block diagram of the DCU is given in Figure 6-1. The high degree of functional redundancy in the design can be observed in the block diagram. It is made up of two identical memory controllers, four identical channel controllers and four nearly identical data buffers in addition to the input/output section, the command/status multiplexer, status memory and bus select logic.

The DCU operates in four configurations: 1) one channel serial, 2) two channel serial, 3) four serial and 4) one channel parallel.

The following sections describe the implementation of the major blocks of the DCU organization.

6.2 MICROPROCESSOR SELECTION

Key components of the DCU are the four microprocessor based channel controllers. Because of this the selection of the microprocessor to be used in this application was a major design decision. An initial comprehensive general survey was made of available devices that included sixteen bit, eight bit and bit slice devices using technology ranging from CMOS to bipolar. Using considerations based on power consumption, available peripheral support devices and development systems, the selection process was narrowed to a selection between the PPS-8, 8080A and 6800. From the standpoint of available peripheral devices and development support equipment, these three devices are essentially equivalent. Thus the decision is resolved to a comparison of performance (speed), required parts count, power consumption and radiation hardness. An assessment of these parameters for the three devices is given below:

Parameter	PPS-8	8080A	6800
Speed	Adequate	Good	Good
Power	Low	30% Higher	30% Higher
Parts	50% Higher	Low	Low
Rad Hardness	Adequate	Poor	Poor

Thus the 8080A and 6800 have an advantage in speed and parts count while the PPS-8 has better power and radiation hardness. After considering these factors it was decided to use the PPS-8 based primarily on the superior radiation hardness supplied by the high voltage PMOS technology used in this device.

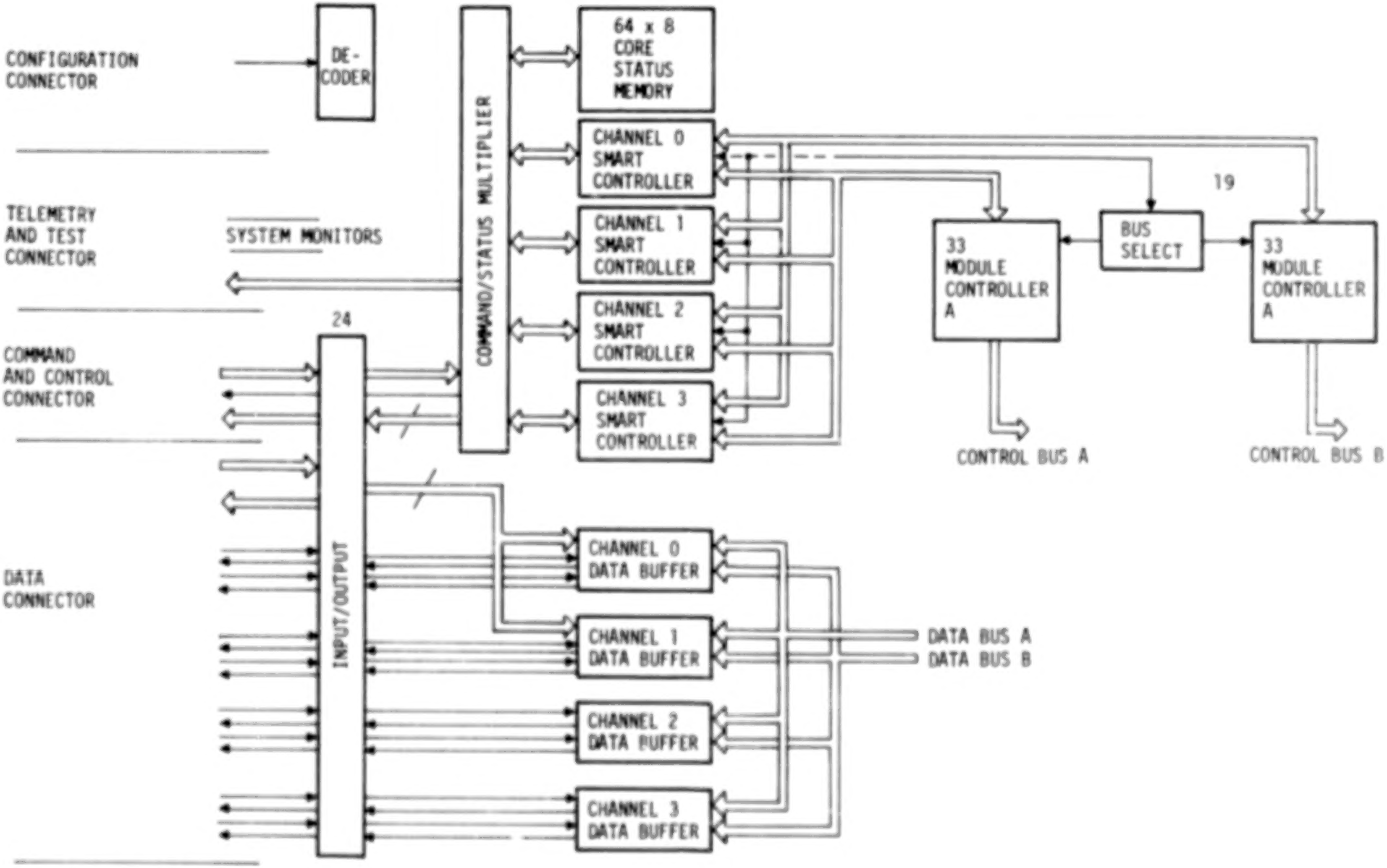

CONFIGURATION CONNECTOR
DE-CODER
64 x 8 CORE STATUS MEMORY
CHANNEL 0 SMART CONTROLLER
CHANNEL 1 SMART CONTROLLER
CHANNEL 2 SMART CONTROLLER
CHANNEL 3 SMART CONTROLLER
COMMAND/STATUS MULTIPLIER
TELEMETRY AND TEST CONNECTOR
SYSTEM MONITORS
19
33 MODULE CONTROLLER A
BUS SELECT
33 MODULE CONTROLLER A
CONTROL BUS A
CONTROL BUS B
24
COMMAND AND CONTROL CONNECTOR
DATA CONNECTOR
INPUT/OUTPUT
CHANNEL 0 DATA BUFFER
CHANNEL 1 DATA BUFFER
CHANNEL 2 DATA BUFFER
CHANNEL 3 DATA BUFFER
DATA BUS A
DATA BUS B

Figure 6-1. Drive and Control Unit Block Diagram

6.3 DATA BUFFER

The combination serial/parallel data buffer shown in Figure 6-2 formats channel serial or 4 bit parallel data as necessary for storage in the DSS. The buffer also decouples data transfers between the channel and DSS to allow fully asynchronous I/O operation with respect to internal SSDR operation. Data are stored in the FIFO buffer until the buffer is ¼ full (empty) during DSS Write (Read) operations. Channels 0 and 1 are the combination serial-parallel data buffers shown. While in the parallel configuration both buffers run simultaneous to achieve the 8 bit wide channel interface.

Channel data buffers 2 and 3 have only the serial ports at the channel interface.

6.4 MEMORY MODULE CONTROLLER

The two identical memory module controllers provide all timing and control to the DSS. They also provide the necessary cycle and data clocks to the DCU channel controllers and data buffers.

The timing and control sequences are determined by the execution of micro code controlled sequences. Each micro-cycle is 138 nsec long which corresponds to 7.5° resolution of DSS field cycle phase for control functions. A block diagram of a controller is given in Figure 6-3. The micro code is stored in the 512 byte programmable ROM.

6.5 BUS SELECT

The bus select logic controls the access of channels to Memory controllers and busses. It arbitrates any conflicts between requesting controllers through priority logic. Within the bus select logic is the 14.4 MHz oscillator which serves as the master clock source for the SSDR.

6.6 CHANNEL CONTROLLER

The block diagram of a single channel controller is given in Figure 6-4. The microcomputer of the channel controller consists of one PPS-8 (P/N 11806), one Clock Generator (P/N 10706), one 256 byte RAM (P/N 10809), three Parallel Data Controllers PCD's, (P/N 10453), and two 4096 byte ROM's (P/N A66F4, A66F5).

6.6.1 Input/Output

The PDC's communicate with eight output "registers" and five input "registers" via LSTTL MSI/SSI circuits. Table 6-1 provides a summary of all I/O registers. Table 6-1 provides the address and program mode of each PDC.

6.6.2 Interrupts

In addition to the automatic Power Clear interrupt, there are nine interrupts implemented in hardware. Each of the nine interrupts is defined below by priority level.

BLANK
PAGE

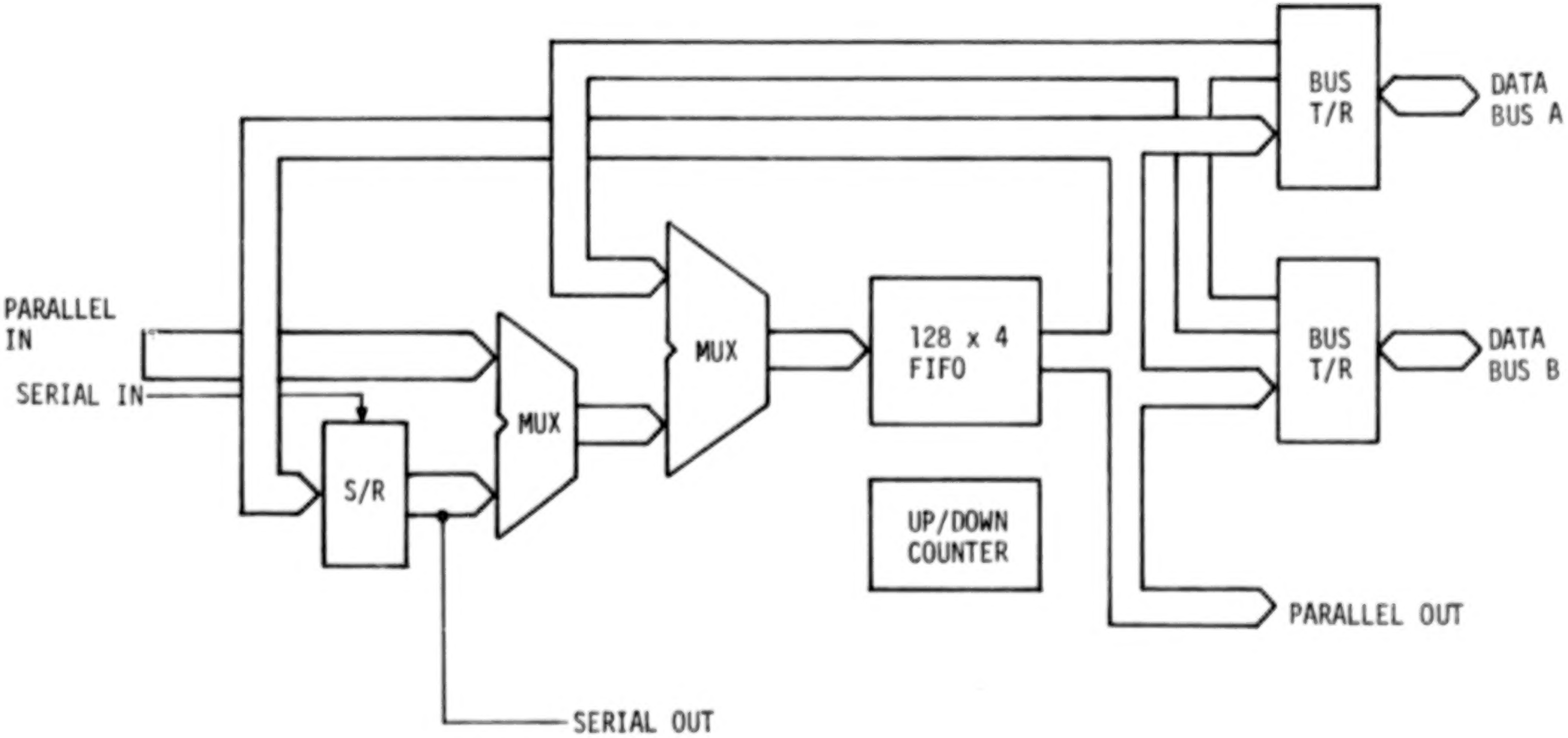

PARALLEL IN
SERIAL IN
S/R
MUX
MUX
128 x 4 FIFO
UP/DOWN COUNTER
BUS T/R
BUS T/R
DATA BUS A
DATA BUS B
PARALLEL OUT
SERIAL OUT

Figure 6-2. Serial/Parallel Data Buffer

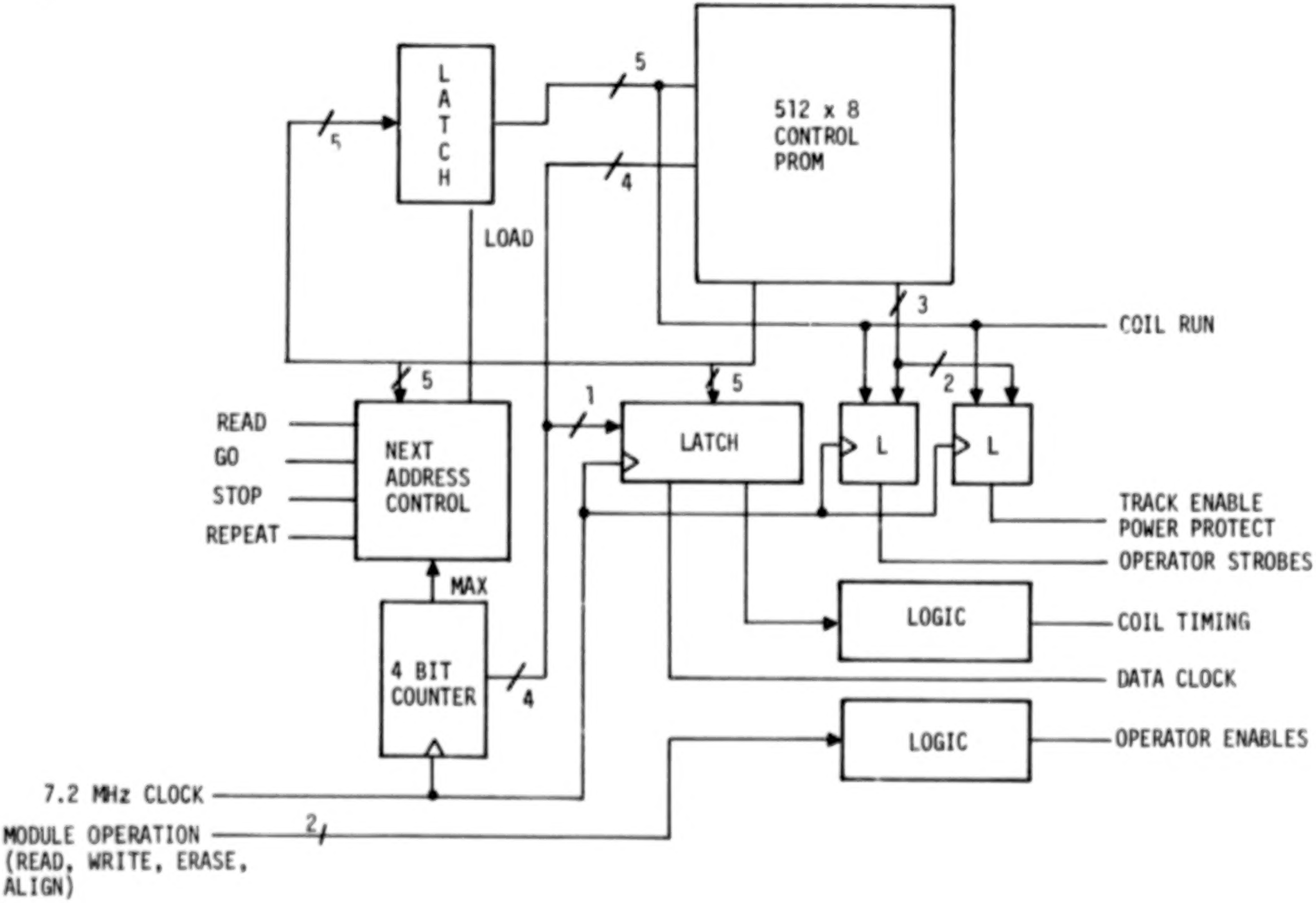

LATCH
5
5
512 x 8
CONTROL
PROM
4
LOAD
3
COIL RUN
5
5
2
1
READ
GO
STOP
REPEAT
NEXT
ADDRESS
CONTROL
LATCH
L
L
TRACK ENABLE
POWER PROTECT
OPERATOR STROBES
MAX
LOGIC
COIL TIMING
4 BIT
COUNTER
4
DATA CLOCK
LOGIC
OPERATOR ENABLES
7.2 MHz CLOCK
MODULE OPERATION
(READ, WRITE, ERASE,
ALIGN)
2

Figure 6-3. Memory Module Controller

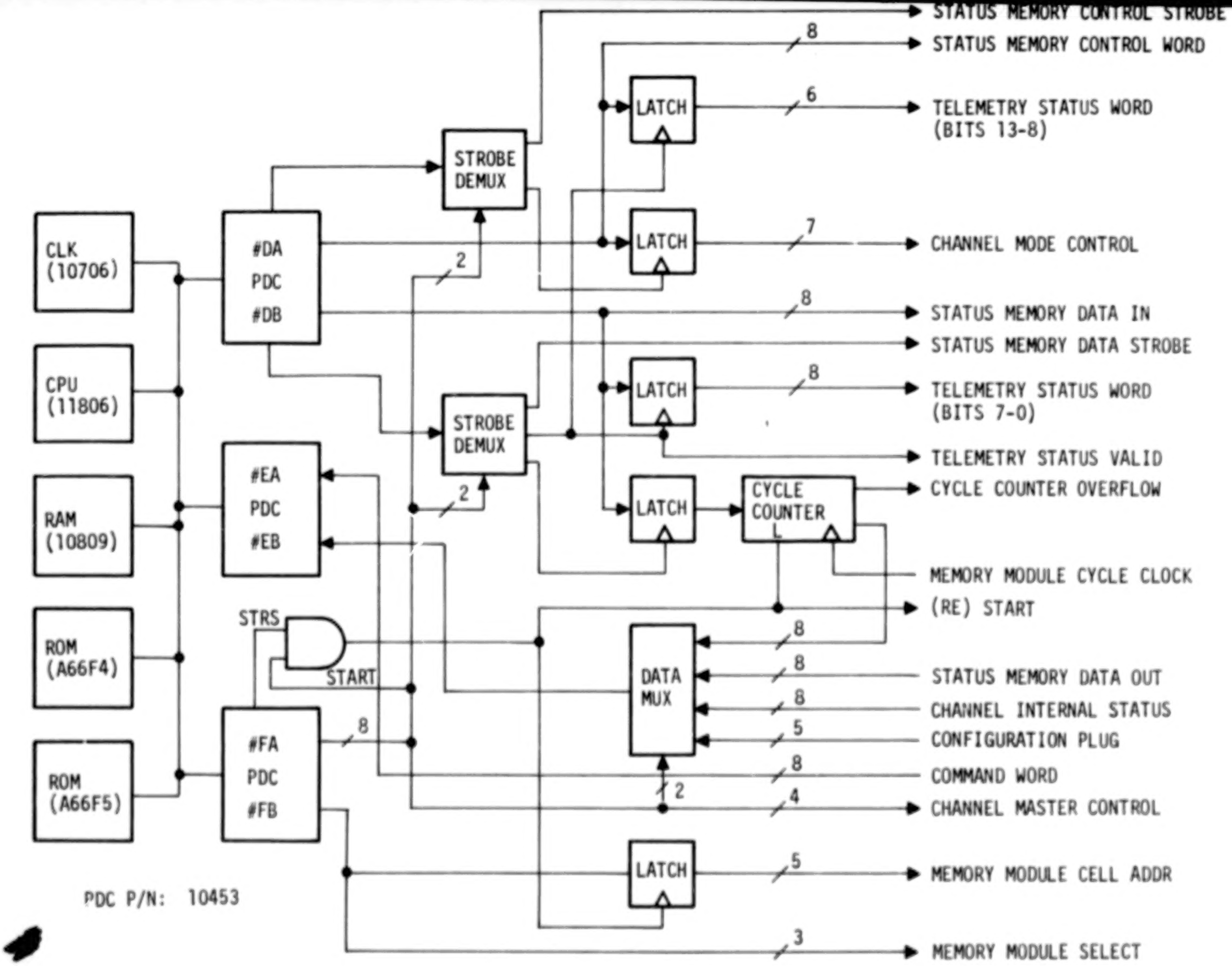

STATUS MEMORY CONTROL STROBE
STATUS MEMORY CONTROL WORD
TELEMETRY STATUS WORD (BITS 13-8)
CHANNEL MODE CONTROL
STATUS MEMORY DATA IN
STATUS MEMORY DATA STROBE
TELEMETRY STATUS WORD (BITS 7-0)
TELEMETRY STATUS VALID
CYCLE COUNTER OVERFLOW
MEMORY MODULE CYCLE CLOCK
(RE) START
STATUS MEMORY DATA OUT
CHANNEL INTERNAL STATUS
CONFIGURATION PLUG
COMMAND WORD
CHANNEL MASTER CONTROL
MEMORY MODULE CELL ADDR
MEMORY MODULE SELECT
CLK (10706)
CPU (11806)
RAM (10809)
ROM (A66F4)
ROM (A66F5)
#DA PDC #DB
#EA PDC #EB
#FA PDC #FB
STROBE DEMUX
STROBE DEMUX
LATCH
LATCH
LATCH
LATCH
LATCH
CYCLE COUNTER
DATA MUX
STRS
START
8
6
7
8
8
8
8
8
8
5
8
4
5
3
2
2
2
8
PDC P/N: 10453

Figure 6-4. Channel Control Block Diagram

Table 6-1. Input/Output Register Summary

µC Reg Name	Source/Destination	Strobe	MSS*	PDC	
				Add'r	Mode
CMCW	Channel Master Control	-	-	FA	CLK Out
MMAW	Memory Module Address	-	-	FB	Static Out
DC	Cycle Counter Out	-	00X	EB	Static In
-	Status Memory Data Out	-	01X	EB	Static In
-	Channel Internal Status	-	10X	EB	Static In
-	Configuration Plug	-	11X	EB	Static In
CWQUE	Command Word	EXEC	-	EA	HS In
-	Cycle Counter Input	CCIS	X00	DB	CLK Out
TMSTAT+1	Telemetry Status, Word 1	TSS1	X01	DB	CLK Out
-	Status Memory Data In	SMDS	X10	DB	CLK Out
CMODE	Channel Mode Control	CMOS	X00	DA	CLK Out
TMSTAT	Telemetry Status, Word 0	TSS1	X01	DA	CLK Out
SMCW	Status Memory Control	SMCS	X10	DA	CLK Out

*Reference CMCW Word Bit Assignment for Definition.

Level 0

Emergency Shutdown (EMSD), INTO, user input used to initiate an immediate orderly shutdown sequence.

Level 1

Buffer Service Request (DBS), INT1, originates from the Channel Data Buffer when service is required.

Level 2.0

Cycle Counter Over Flow (CCOF), FCA2, occurs whenever the 8 bit cycle counter overflows.

Cell Stopped (CSPD), FCB2, occurs whenever propagation in the active cell is stopped.

Bus Request Acknowledge (BRA), FCB1, occurs whenever a buffer service request has been acknowledged.

Level 2.1

Execute (EXEC), ECA2, a user input indicating the presence of a valid command in PDC EB.

Data Buffer Empty (DBE), ECB1, occurs when the Channel Data Buffer becomes empty if Input Enable (IE) is reset.

Level 2.2

Status Memory Acknowledge (SMAK), DCA2, occurs to ackowledge the status memory request by the channel.

Interlock (INLK), DCB2, a user input authorizing an "all channel" command.

Of the nine hardware interrupts, three are enabled by the program. They are: Emergency Shutdown, Buffer Service Request and Cycle Counter Overflow.

6.7 STATUS MEMORY

The status memory is a 64 word by 8 bit memory system capable of operating in the read/restore or clear/write modes at a cycle time of 12 microseconds. The magnetics is a 3 wire 2½ D organization wired as a 512 word by 1 bit array containing decoding diodes. The ferrite core is an 18 mil low drive,420 ma full drive over temperature (Ampex Part #324 1738-20).

6.7.1 Description

The system electronics can be divided into three categories: the core array and drive circuits, system timing, and power control. A block diagram is given in Figure 6-5. Each axis is driven by four dual memory driver/switches (SN 55325) with selection provided by two SN54LS139 (dual 2 to 4 line decoder). The selection of a source and sink in the "A" axis will provide a current path through 32 cores. The direction of current is determined by four gates in the system timing section. This current is

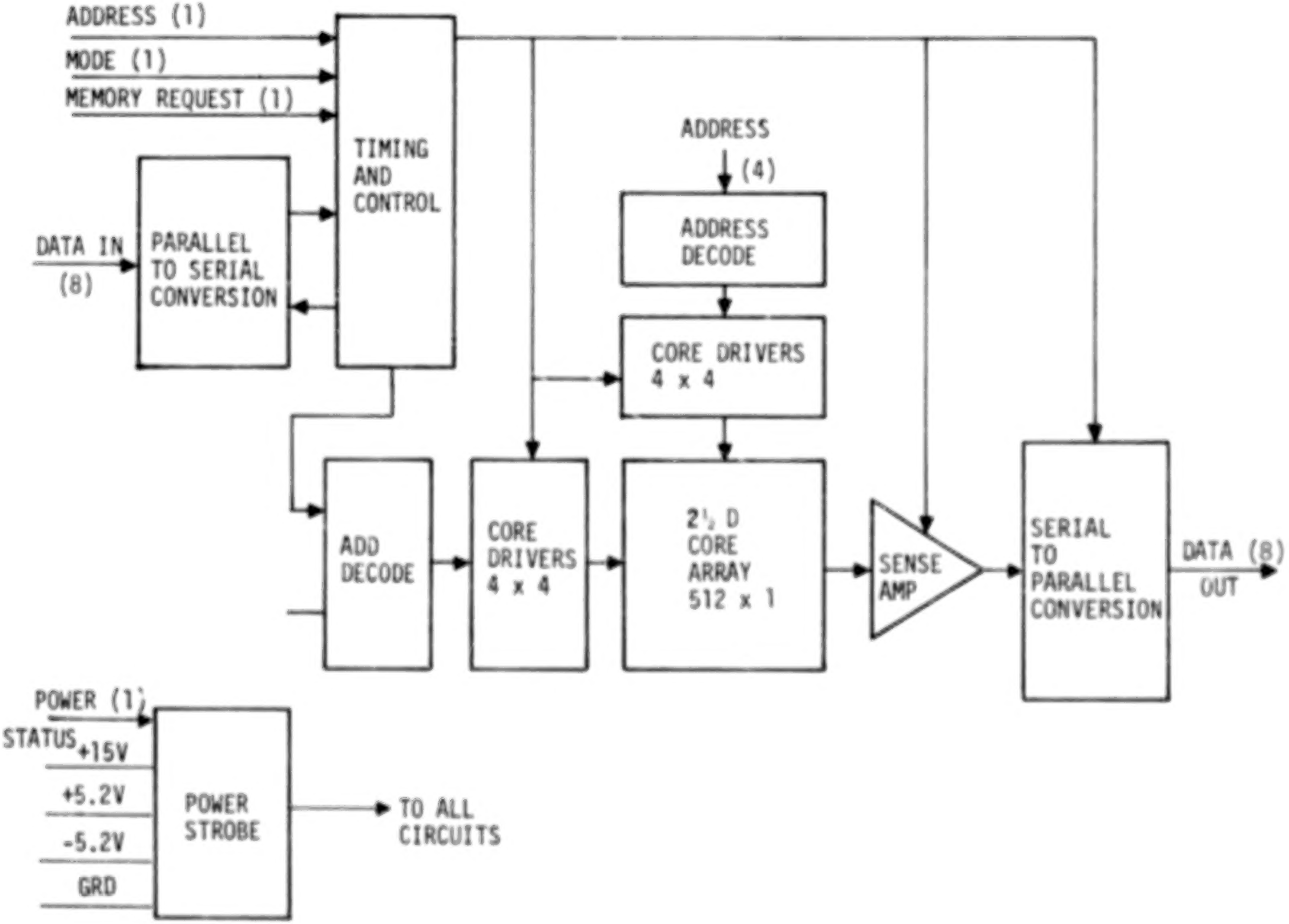

ADDRESS (1)
MODE (1)
MEMORY REQUEST (1)
TIMING AND CONTROL
DATA IN (8)
PARALLEL TO SERIAL CONVERSION
ADDRESS (4)
ADDRESS DECODE
CORE DRIVERS 4 x 4
ADD DECODE
CORE DRIVERS 4 x 4
2½ D CORE ARRAY 512 x 1
SENSE AMP
SERIAL TO PARALLEL CONVERSION
DATA (8) OUT
POWER (1)
STATUS
+15V
+5.2V
-5.2V
GRD
POWER STROBE
TO ALL CIRCUITS

Figure 6-5. Status Memory

equal to ½ full drive current. A similar selection in the "Y" axis will provide ½ full drive current through 32 cores. However, 16 of the cores will see a positive current and 16 cores will see a negative current. This technique is called re-entry. The summation of currents will switch one core and disturb the other. The selection of "Y" source and sink circuit can change direction of "Y" currents, thereby permitting writing or reading in both halves of the stack.

6.7.2 Status Memory

The timing and control output consists of four input gates (current phase gates) used to establish timing, read, write, and polarity of drive currents. The "Y" drive polarity is determined by address bit (A_{OB}), causing either coincident or anti-coincident reading or writing in the array. The mode term "M" controls the read/restore and clear/write operations. When the mode term is high, a read/restore operation will be performed. Data from the sense amplifier is directed to the current phase gate which selects the source/sink array drivers. When the mode term is low, a clear/write operation is performed. During writing, data from the input shift register controls the current phase gate. The X, Y timing is generated by a monostable multivibrator (one shot).

The memory request pulse is detected by a SN54121 (one shot) which clears/loads all data address registers and counters. The half cycle pulse (HC) is generated from the clear pulse. The train of pulses HC, EC, and ECS once stared continues by way of feedback of $\overline{\text{ECS}}$ to the HC one shot. A counter, SN54161, counts 8 pulses, then inhibits the HC one shot. This completes one word of memory of 8 bits. A memory request and address data must be generated to start a new cycle. One word of memory requires 11.4 μsec to complete. A total of 64 cycles is required to write the full memory. The terms M, HC, and X, Y timing clock data into the output shift register SN54LS164. The term ECS clocks input data to the write gate. The input data register is a parallel to serial converter. The output shift register is a serial to parallel converter. Reading or writing a single bit at a time reduces the number of sense amplifiers required to one. The single sense amplifier (SN55234) senses the array (single sense winding) and sets the SN54LS74 F/F which is strobed. Data is sent to the output shift register and to the current phase gate which rewrites the data into the array for the read/restore operation.

6.8 DCU CHANNEL OPERATION

6.8.1 Operating Modes

While the SSDR is in operation, each active channel is in one of five operating modes including Standby. There are three submodes of Standby. The state of the Channel Ready and Data Valid flags is given in the mode description which follows as appropriate.

Erase - While in the Erase mode, consecutive storage locations are cleared of any previous data. Erasure occurs at the maximum rate (50% Memory Module duty cycle) in increments of sixteen bits independent of the channel data clock input. The Channel Ready and Data Valid flags are FALSE.

Write - While in the Write mode, data present at the input are loaded into the channel data buffer at the user clock rate whenever the Data Valid flag is TRUE. The data buffer contents are written into consecutive channel storage locations in sixteen bit increments at the rotating field rate. Storage locations are simultaneously cleared of any previous stored data. The Channel Ready flag is FALSE.

Read - While in the Read mode, consecutive storage locations are read into the channel data buffer in sixteen bit increments at the rotating field rate. Data are transferred to the channel data output line(s) at the user clock rate whenever the Data Valid flag is TRUE. The Channel Ready flag is FALSE. Store contents are not altered.

Align - While in the Align mode, storage locations are moved in sixteen bit increments at the maximum rate (50% Memory Module duty cycle) independent of the channel data clock. Stored contents are not altered. The Channel Ready flag is FALSE.

Standby - While in the Standby mode, the channel is idle and the Channel Ready flag is TRUE. Any output data remaining in the data buffer at the conclusion of an operation may be removed at the user clock rate. The Data Valid flag is TRUE if such residual data are present, otherwise, the Data Valid flag is FALSE. The three submode of Standby are Read Standby, Write Standby and Reset Standby. While in Read Standby, the last cell read is aligned to the Read Pointer (RP) and all other cells are aligned to the beginning-of-cell (BOC). While in Write Standby, the last cell written into is aligned to the Write Pointer (WP) and all other cells are aligned to the beginning-of-cell. While in Reset Standby, all cells are aligned to the beginning-of-cell. Current channel status is present in the Status Memory while in a standby mode.

6.8.2 Command Set

The operation of a SSDR channel is determined by commands issued via an 8-bit command word, an Execute line and an Interlock line. Unless otherwise mentioned, a command will be executed only if the selected channel is in a standby mode. If the "all channel" flag (A) is set, all channels, if in the required mode, execute the command. Telemetry status for the specified channel N is continuously updated and output as part of a command operation except for the Read and Write commands. For these two commands telemetry status is output at the beginning and at the end of the operation.

"All channel" commands require an Interlock line transition to be recognized. The most recently received command has priority over all prior commands. Unless otherwise defined, the command word length is one byte.

Erase (A,N) - When received, the channel N data buffer is cleared, the Align mode entered and the storage is aligned to the beginning-of-storage (BOS). The Erase mode is entered and erasure begins at the channel BOS or at MEA zero of the first functional cell thereafter. Unless a STOP (A,N) or RESET (A,N) command is received, erasure of each functional cell continues to the end-of-storage (EOS), at which time all channel pointers are set to BOS and the Reset Standby submode entered.

Write (A,N) - If "Channel Full" (CFULL) flag is set the write command is ignored. The initial write command response is Standby submode dependent as defined below.

a. Read Standby: The channel N data buffer is cleared, the Align mode entered and the cell specified by the RP is realigned to the BOC. Storage is aligned to the WP and the Write mode entered. If WP = RP, the realign and align operations are bypassed.

b. Reset Standby: The channel N data buffer is cleared, the Align mode is entered, storage is aligned to the WP and the Write mode entered.

c. Write Standby: The channel N data buffer is cleared and the Write mode is entered.

Unless otherwise commanded, while in the Write mode, writing proceeds through each consecutive functional cell until EOS is reached. At this time, the data buffer is cleared, the WP is set to BOS, the CFULL flag is set and the Reset Standby submode is entered.

Read (A/N) - If WP = RP (PEFLG set) and CFULL is not set, the Read command is ignored. Initial Read command response is Standby submode dependent as defined below.

a. Write Standby: The channel N data buffer is cleared, the Align mode is entered and the cell specified by the WP is realigned to BOC. Storage is aligned to the RP and the Read mode is entered. If WP = RP, and CFULL is set, the Align mode operations are bypassed.

b. Reset Standby: The channel N data buffer is cleared, the Align mode is entered, storage is aligned to the RP and the Read mode entered.

c. Read Standby: The channel N data buffer is cleared and the Read mode entered.

Unless otherwise commanded, while in the Read mode, reading proceeds through each consecutive functional cell until the WP or the EOS is reached. If the WP is reached, reading stops and the Write Standby mode is entered. If CFULL is set, reading proceeds until the EOS is reached at which time reading stops and the Reset Standby mode is entered.

Go To Write (N,X) - Initial channel response is dependent on the present mode as defined below. Cell functional status is ignored. Go to Write is a two byte command word. Cell X is not required to be within the storage allocated channel N.

a. Write Standby: The channel N data buffer is cleared, the Align mode is entered and the cell specified by the WP is realigned to BOC.

b. Read Standby: The channel N data buffer is cleared, the Align mode is entered and the cell specified by the RP is realigned to BOC.

c. Reset Standby: The channel N data buffer is cleared.

The Write mode is entered and writing begins at BOC and continues until the EOC is reached unless a STOP (N) or RESET (N) command is received. When the EOC is reached, the Data Valid flag is set FALSE and the data buffer cleared and the Reset Standby mode is entered. The read and write pointers are not altered by the Go To Write Command.

Go To Read (N,X) - The command is recognized and executed when channel N is in a Standby submode. Initial response is dependent on the present mode as defined above for the Go To Write command. The Read mode is entered and reading begins at BOC and continues until the EOC is reached unless a STOP (N) or RESET (N) command is received. When the EOC is reached, reading into the data buffer is stopped and the Reset Standby mode is entered.

As with the Go To Write command, the Go To Read command also ignores cell functional status and has a length of two bytes. In addition, cell X is not required to be within the storage allocated channel N. The read and write pointers are not affected by the Go To Read command.

Stop (A, N) - The command is recognized and executed whenever the channel is in a mode other than Align. Response is as defined below for each mode:

a. Erase: Erasure is halted at the EOC. All channel pointers set to BOS and the Reset Standby mode entered.

b. Write: If in the Write mode due to a Write command, the Data Valid flag is set FALSE and residual data in the data buffer is written into storage. The WP is saved and the Write Standby mode entered.

   If in the Write mode due to a Go To Write command, the Data Valid flag is set FALSE and residual data in the data buffer is written into storage. The Align mode is then entered and cell X is realigned to the BOC. The channel then enters the Reset Standby mode.

c. Read: If in the Read mode due to a Read command, reading from storage is stopped, the RP is saved and the Read Standby mode entered.

   If in the Read mode due to a Go To Read command, reading is stopped and the data buffer is cleared. The Align mode is entered and cell X is realigned to the BOC. The channel then enters the Reset Standby mode.

Upon entering the appropriate standby mode, the present channel status is transferred to the SSDR status memory.

Read Restart (A,N) - If the channel is in the Read Standby mode, the Align mode is entered and storage is realigned to the BOS. The RP is set to BOS. The data buffer is cleared and the Reset Standby submode is entered. If in the Write Standby or Reset Standby submodes, the RP register is set to the BOS. Channel mode is not otherwise affected. Channel status is transferred to the status memory.

Reset (A,N) - The command is recognized and executed by channel N from any mode other than Align. The configuration plug is read and the configuration is re-established. The first functional cell is determined. The data buffer is cleared and all pointers are set to BOS and all flags initialized. The Reset Standby mode is entered and the present channel status transferred to the status memory.

Set Read (N,X,SMEA) - When received, the channel N data buffer is cleared, the Align mode entered and storage aligned to the BOC. The read pointer set to X, SMEA and Reset Standby entered. Channel status is transferred to the status memory. The write pointer is not affected. The "pointers equal" flag is serviced. Set Read is a five byte command word.

Set Write (N,X, SMEA) - When received, the channel N data buffer is cleared, the Align mode entered and storage aligned to the BOC. The write pointer set to X, SMEA and Reset Standby entered. Channel status is transferred to the status memory. The read pointer is not affected. BOS and Channel FULL flags are serviced. Set Write is a five byte command word.

Skip Set (N,X) - The bit of the functional status register specified by X is set in both the channel RAM and the status memory. At the conclusion of the command, the channel will return to the Standby mode. The specified cell or controller will no longer be used except for a Go To command. Skip Set is a two byte command word.

Skip Reset (N,X) - The operation parallels the Skip Set command, but resets the functional status bit specified by X to allow the cell or controller to be returned to normal service. Skip Reset is a two byte command word.

Status (T, N) - There are two types of Status commands. The type I command causes the 14 telemetry status indicator flags to be simultaneously updated. Type II commands cause internal channel status registers' contents to be sent, eight bits per word, in a predetermined sequence. The format is identical to the channel status memory data format.

Recorder Off - The command is an all channel command. All secondary voltages are removed.

Emergency Shutdown - The emergency shutdown command is an all channel command received on a separate control line, rather than as a command word. When a positive transition occurs on this line, all operation is halted for all channels. Each channel not in Standby transfers the internal status registers' contents to the core status memory. At the completion of the transfers, all secondary voltages are removed.

Recorder On - The Recorder On command is an all channel command received on a discrete control line. When received, secondary voltages are applied and the contents of Status Memory are transferred to the Channel Controller RAM allowing the recorder to resume operation as established prior to the recorder OFF command. If recorder ON is applied in conjunction with the initialization (INITZ), the channel is initialized to a reset state and reset standby entered.

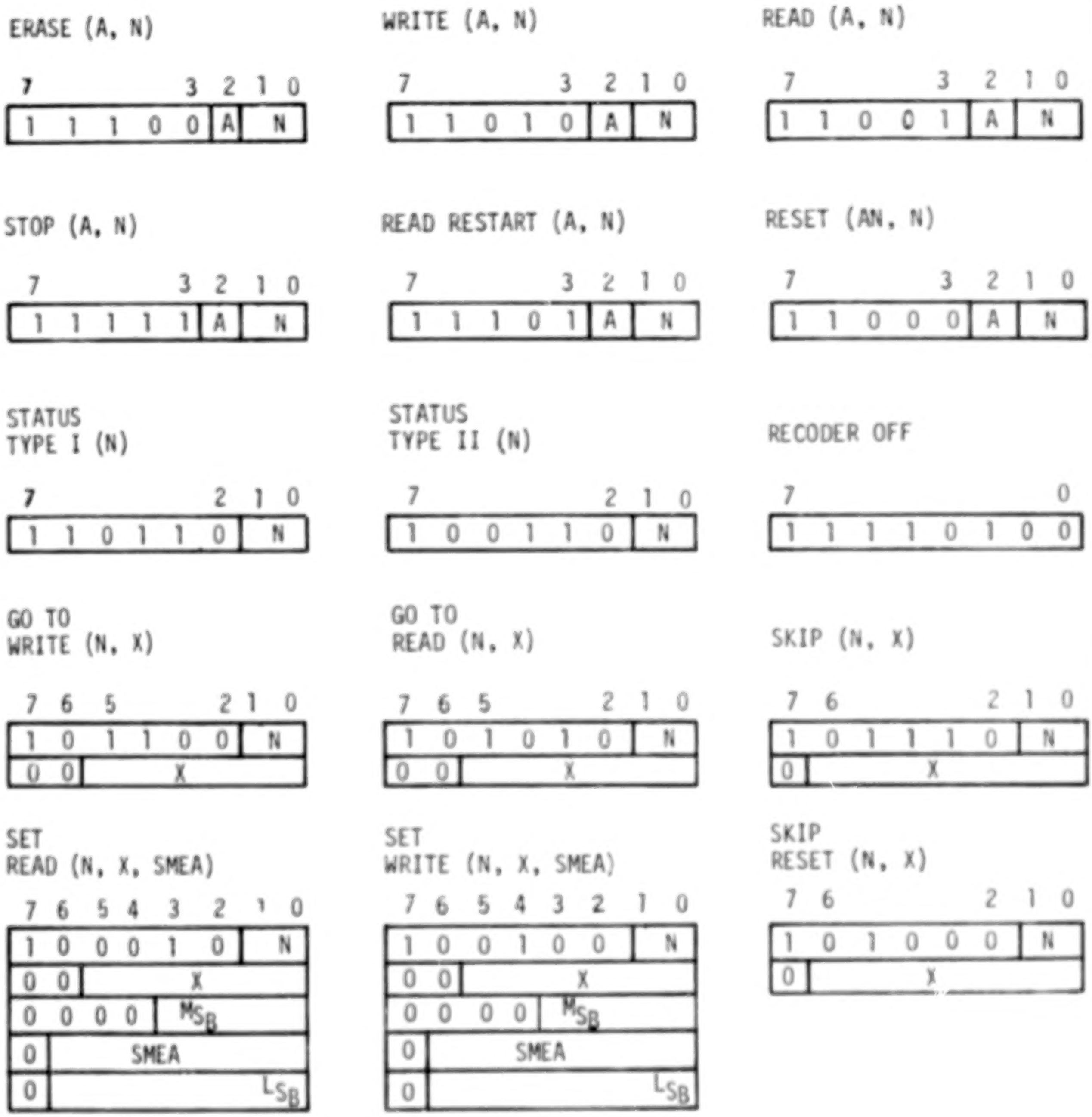
6.9 REGISTER FORMATS

6.9.1 Command Word Coding

The coding of all bytes of the 14 recorder command words is given in Figure 6-6.

6.9.2 Operating Status Registers

The operating state of each channel is contained in RAM in the following status registers when the SSDR is on. The register contents are transferred to the core status memory when entering the Standby mode or as the result of an Emergency Shutdown prior to the removal of power from the SSDR.


ERASE (A, N)
7 3 2 1 0
1 1 1 0 0 A N
WRITE (A, N)
7 3 2 1 0
1 1 0 1 0 A N
READ (A, N)
7 3 2 1 0
1 1 0 0 1 A N
STOP (A, N)
7 3 2 1 0
1 1 1 1 1 A N
READ RESTART (A, N)
7 3 2 1 0
1 1 1 0 1 A N
RESET (AN, N)
7 3 2 1 0
1 1 0 0 0 A N
STATUS TYPE I (N)
7 2 1 0
1 1 0 1 1 0 N
STATUS TYPE II (N)
7 2 1 0
1 0 0 1 1 0 N
RECODER OFF
7 0
1 1 1 1 0 1 0 0
GO TO WRITE (N, X)
7 6 5 2 1 0
1 0 1 1 0 0 N
0 0 X
GO TO READ (N, X)
7 6 5 2 1 0
1 0 1 0 1 0 N
0 0 X
SKIP (N, X)
7 6 2 1 0
1 0 1 1 1 0 N
0 X
SET READ (N, X, SMEA)
7 6 5 4 3 2 1 0
1 0 0 0 1 0 N
0 0 X
0 0 0 0 MSB
0 SMEA
0 LSB
SET WRITE (N, X, SMEA)
7 6 5 4 3 2 1 0
1 0 0 1 0 0 N
0 0 X
0 0 0 0 MSB
0 SMEA
0 LSB
SKIP RESET (N, X)
7 6 2 1 0
1 0 1 0 0 0 N
0 X

A: "ALL CHANNEL" FLAG

N: CHANNEL NUMBER, 0, 1, 2, 3

X: CELL ADDRESS, 0, ..., 63 FOR CELLS; MEMORY CONTROLLER; 64 FOR CONTROLLER A, 65 FOR CONTROLLER B (SKIP AND SKIP RESET)

SMEA: MEMORY ELEMENT ADDRESS, -102144_{10} TO 255_{10}

Figure 6-6. Command Word Coding

Telemetry status (TMSTAT) - 16 bits contain the present channel status. The format is as follows:

TMS <15-11> - Present Channel Mode
TMS < 10 > - RP = WP Flag (PEFLG)
TMS < 9 > - BOS Flag (BOS FG)
TMS < 8 > - Channel Full Flag (CFULL)
TMS < 7-2 > - Active Cell Address (X)
TMS < 1-0 > - Channel Number (N)

Channel Status Flag Word (CSFW) - 8 bit word provides channel operations status flags defined in the program listing.

Present Pointer (PP) - 24 bits contain the present cell address (PX) and the present count (PC) of the memory element address (MEA). Cell address, PX, and PC fields are 6 and 18 bit fields respectively. The PC is a two's complement number biased by -102,144. PC = -102,144 when MEA = BOC.
PC = +255 when MEA = EOC.

Write Pointer (WP) - 24 bits contain the cell address and memory element address of the next storage location to be written into during a normal write operation. Register format is also identical to PP format.

Read Pointer (RP) - 24 bits contain the cell address and memory element address of the next storage location to be read during a normal read operation. Register format is identical to PP format.

Memory Module Controller Status (MMCSTAT) - 2 bits provide the functional status of Memory Module Controllers A and B.

6.9.3 Functional Status

The functional status (failed or working) of the 64 memory cells and the two memory module controllers are contained in 66 flags. Duplicate copies of these 66 one bit flags are contained in both RAM and the core status memory. These flags are individually set and reset by the respective Skip and Skip Reset commands. They are read from status memory during the recorder turn-on sequence.

6.9.4 Status Memory Map

Figure 6-7 provides a map of the 64 byte status memory. The operating status of individual chnnels is as defined above.

6.9.5 Telemetry Status

The format of the 14 bit Type I telemetry status word is as defined under Operating Status Registers above as TMS <13-0>. The Type II telemetry status consists of 12 TMS words. TMS bits 13-11 are uniquely coded to identify the status word (i.e., word address). TMS <7-0> are a byte of status of the 12 bytes of channel operating status registers defined above exclusive of the Memory Module Controller Status Register.

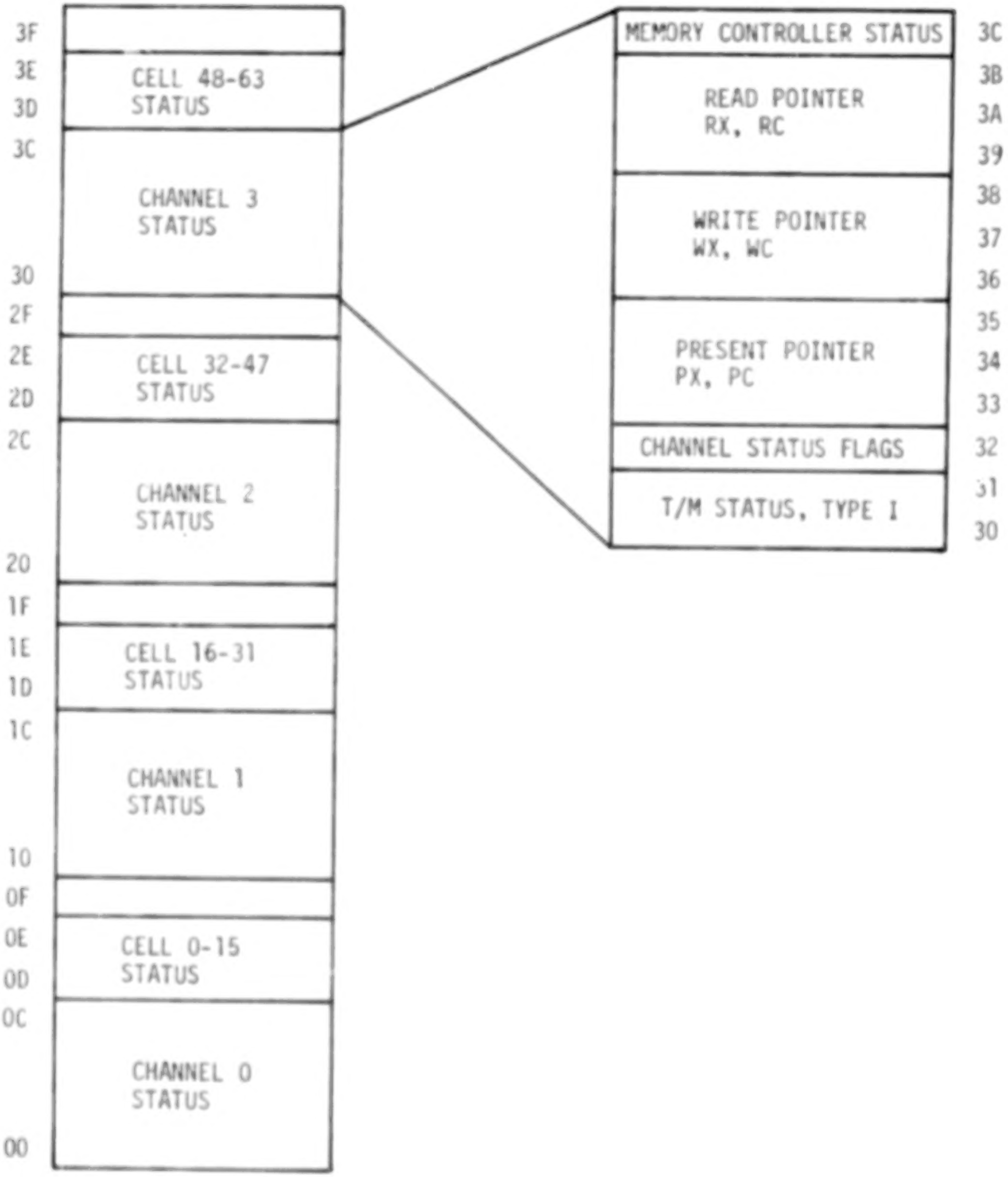

3F
3E
3D
CELL 48-63 STATUS
3C
CHANNEL 3 STATUS
30
2F
2E
2D
CELL 32-47 STATUS
2C
CHANNEL 2 STATUS
20
1F
1E
1D
CELL 16-31 STATUS
1C
CHANNEL 1 STATUS
10
0F
0E
0D
CELL 0-15 STATUS
0C
CHANNEL 0 STATUS
00
MEMORY CONTROLLER STATUS
3C
3B
3A
READ POINTER RX, RC
39
38
37
WRITE POINTER WX, WC
36
35
34
PRESENT POINTER PX, PC
33
32
CHANNEL STATUS FLAGS
31
T/M STATUS, TYPE I
30

Figure 6-7. Status Memory Map

7.0 POWER SUPPLY

7.1 INTRODUCTION

The SSDR Power Supply Module (PSM) accepts the 28 volt D.C. primary power and generates the secondary voltages necessary for operation of the memory. In establishing a design approach for the power supply, weight, volume and efficiency were primary considerations. These requirements lead to use of a switching regulator custom designed to meet the specific power and packaging requirements of the SSDR. A specification was generated for such a power supply and estimates obtained for design and development. The cost, mainly because of stringent packaging requirements, was significant. Since the power supply was judged to be noncritical to the overall program objective of establishing feasibility of bubble technology, it was decided to use a more cost effective though less efficient approach to the power supply requirement. The approach selected was to utilize standard, commercially available, power supply modules configured to meet the SSDR power requirements and mounted in a chassis compatible with the overall SSDR mechanical design.

7.2 POWER SUPPLY REQUIREMENTS

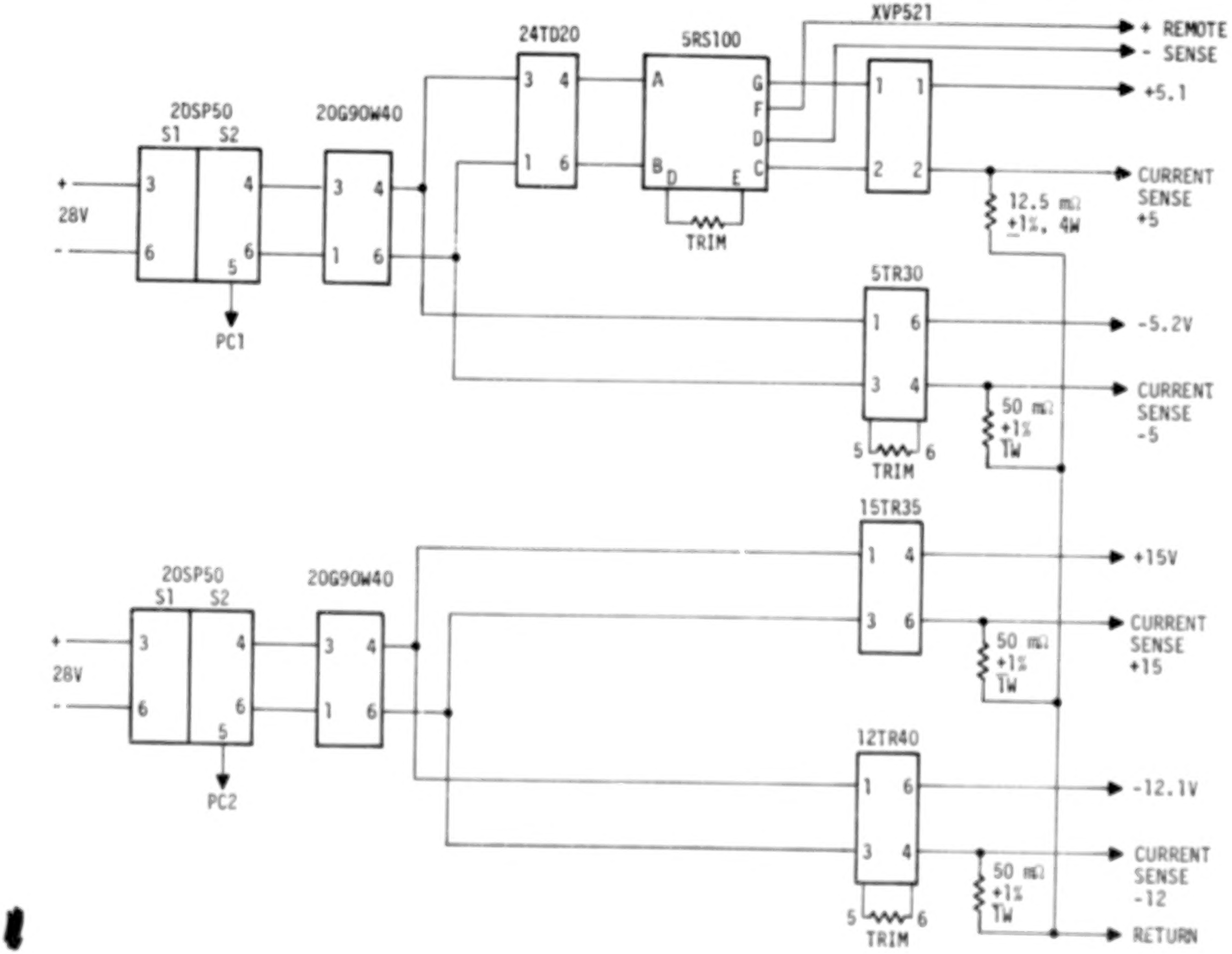
Based on the designs for the Memory Module and DCU, voltage levels, current levels and regulation requirements were established for the power supply. This power supply specification is summarized in the table below.

Voltage	Peak Current	Regulation
+60V	2A	≤3%
+15V	6A	≤3%
-5.1V	8A	≤3%
-5.2V	1A	≤5%
-12.1V	1.7A	≤4%

The +5.1V, -5.2V and -12.1V supplies are offset from their nominal values to take into account the voltage drops developed through the power switches used in the SDDR circuitry to minimize power consumption. In addition to providing power, the power supply provides circuitry for turning the power supply on from a nominally zero power off state. The supply also generates analog signals proportional to the current level in each supply for system status monitoring.

7.3 POWER SUPPLY DESIGN

The power supply design was implemented using commercially available Powercube Cirkitblock Modules. A block diagram of the supply is given in Figures 7-1 and 7-2. The low voltages of Figure 7-1 are generated by first applying the 28 volt primary power to two 20SP50 switching preregulators which



XVP521
+ REMOTE
- SENSE
24TD20
5RS100
+5.1
20SP50
S1
S2
20G90W40
CURRENT
SENSE
+5
+
28V
-
12.5 mΩ
±1%, 4W
TRIM
PC1
5TR30
-5.2V
CURRENT
SENSE
-5
50 mΩ
±1%
1W
TRIM
15TR35
+15V
20SP50
S1
S2
20G90W40
CURRENT
SENSE
+15
50 mΩ
±1%
1W
PC2
12TR40
-12.1V
CURRENT
SENSE
-12
50 mΩ
±1%
1W
TRIM
RETURN

Figure 7-1. Power Supply Block Diag am

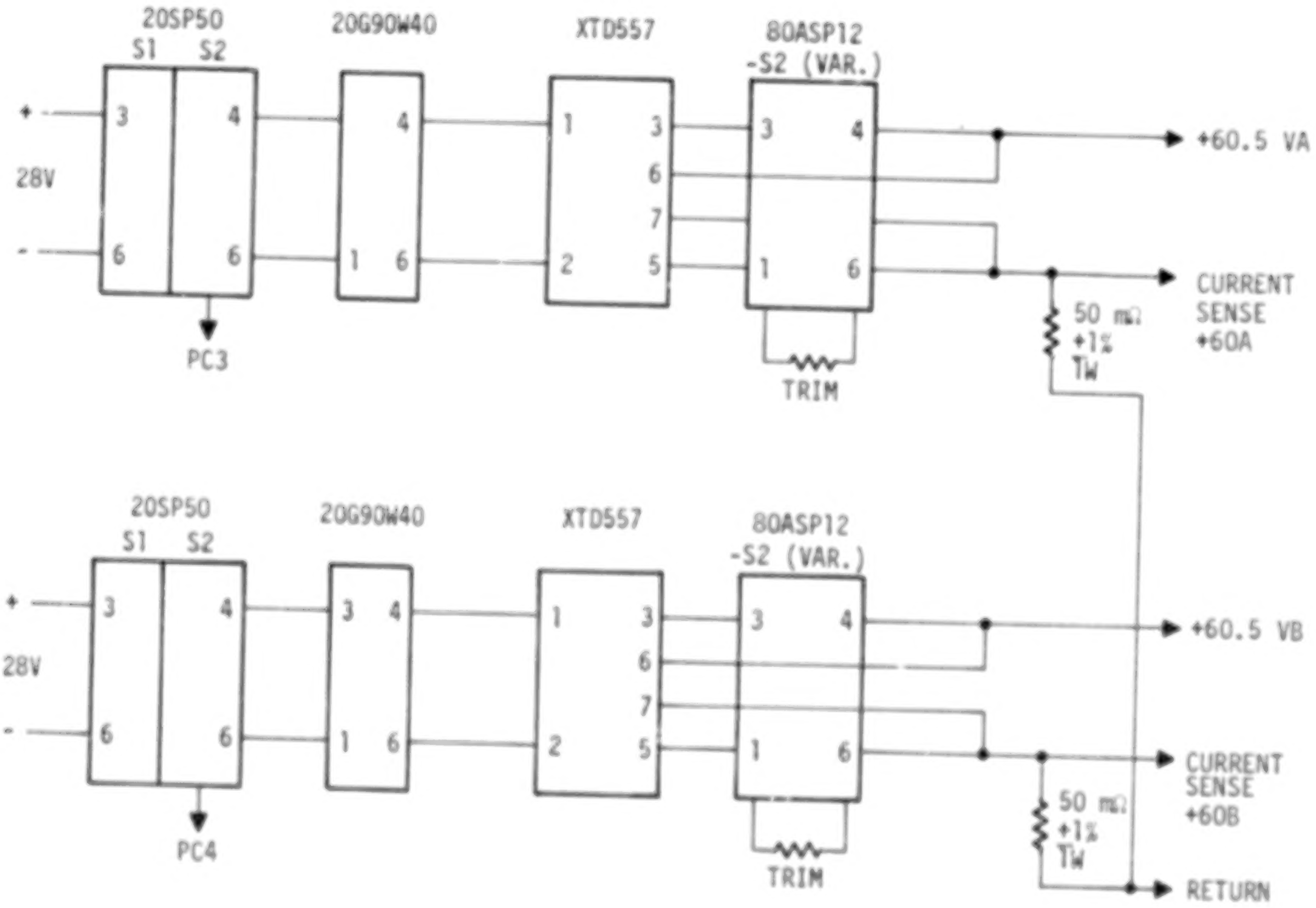

20SP50
S1
S2
20G90W40
XTD557
80ASP12
-S2 (VAR.)
+
28V
-
3
4
6
1
2
5
7
PC3
TRIM
+60.5 VA
CURRENT
SENSE
+60A
50 mΩ
±1%
TW
20SP50
S1
S2
20G90W40
XTD557
80ASP12
-S2 (VAR.)
PC4
TRIM
+60.5 VB
CURRENT
SENSE
+60B
50 mΩ
±1%
TW
RETURN

Figure 7-2. Power Supply Block Diagram

convert the input voltage to a tightly regulated nominal 20 volt D.C. level. The output of both preregulators is then converted to a 40 volt A.C. signal by the two 20G90W40 high frequency generators. One of these high frequency generators drives the 15TR35 and 12TR40 regulator modules to provide the +15 and -12.1 volt levels. The second high frequency generator drives a 5TR30 regulator module to provide the -5.2 volts and also drives a 24TD20 unregulated output module which generates an unregulated 24 volts at its output. This voltage is then provided to the 5RS100 switching regulator which generates the +5.1 volts. The XVP521 is an overvoltage crowbar protection circuit.

The high voltage supply of Figure 7-2 consists of two identical regulators which independently supply the two memory modules. The 60 volt regulator consists of a 20 volt switching preregulator (20SP50), a 20G90W40 40 volt high frequency generator, a XTD557 80 volt unregulated output module and a 80ASP12-52 switching regulator which provides the 60 volts.

Power supply control functions are provided by the two circuits of Figure 7-3 and 7-4. The ON/OFF controller of Figure 7-3 provides the interface by which the SSDR is turned on and off. When 28 volts is initially applied, the terms PC1 through PC4 will rise to 5 volts and act as disable terms to the power supply preregulators. Capacitor C4 limits rise time of the applied voltage to prevent turn on of the latch consisting of Q4 and Q5. When the recorder-on control, ROC, is brought to +5 volts, C1 begins to charge until it reaches a threshold level of 3 volts where the latch consisting of Q1 and Q2 fires-applying a pulse to transformer T1 which is coupled to the Q4, Q5 latch to turn it on. This takes the control terms PC1-PC4 to ground and enables the power supply. SSDR turn-off is achieved by a negative going transition of the OFF signal. The pulse couples through the transformer and turns the Q4, Q5 latch off.

The power supply also contains a power operate (POP) generator which provides a signal which indicates power levels are up and stabilized and recorder operation may be initiated. This circuit is illustrated in Figure 7-4. Circuit operation is initiated when the 5.1 volt supply (Input C) reaches about three volts and Q15 is turned on. This initiates charging of timing capacitor C6. When the timing capacitor voltage reaches the reference voltage from CR16, comparator Q13 and Q14 fires turning Q16 on and generating the POP signal.

The overall power supply design was established to meet the EMI design goals for the SSDR. This was done by packaging the power supply in a totally enclosed chassis using EMI feedthroughs on input and output lines.

All voltages are provided as analog signals at the telemetry connector J4. These voltages are provided with a source impedance of 1 KΩ ± 1%. In addition, current sensing is provided by analog voltage signals at this connector. These signals are generated by low resistance current sensing resistors in the ground leg of the power supply. (See Figures 7-1 and 7-2) scale factors for these sensing functions are summarized as: +60.5 Volts A - 20 ma/mV - coil drive, +60.5 Volts B - 20 ma/mV - coil drive, +5 Volts - 80 ma/mV, -12 Volts - 20 mA/mV, -5 Volts - 20 ma/mV.

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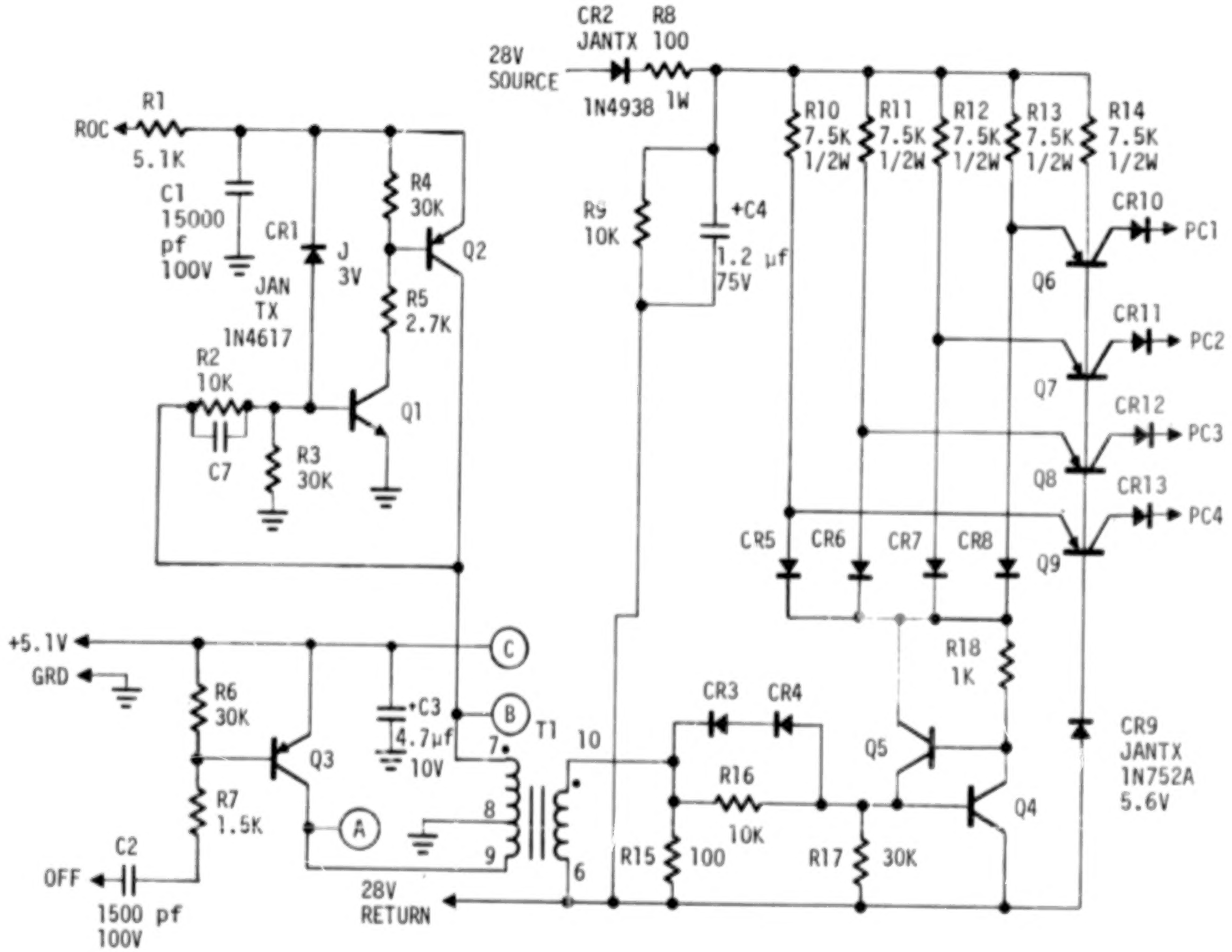
ROC
R1
5.1K
C1
15000
pf
100V
CR1
J
3V
JAN
TX
1N4617
R4
30K
Q2
R5
2.7K
R2
10K
Q1
C7
R3
30K
+5.1V
GRD
R6
30K
Q3
R7
1.5K
C2
1500 pf
100V
OFF
+C3
4.7µf
10V
A
B
C
T1
7
8
9
10
6
28V
RETURN
28V
SOURCE
CR2
JANTX
1N4938
R8
100
1W
R9
10K
+C4
1.2 µf
75V
R10
7.5K
1/2W
R11
7.5K
1/2W
R12
7.5K
1/2W
R13
7.5K
1/2W
R14
7.5K
1/2W
CR10
PC1
Q6
CR11
PC2
Q7
CR12
PC3
Q8
CR13
PC4
Q9
CR5
CR6
CR7
CR8
R18
1K
CR3
CR4
R16
10K
R15
100
R17
30K
Q5
Q4
CR9
JANTX
1N752A
5.6V

Figure 7-3. On/Off Power Supply Controller

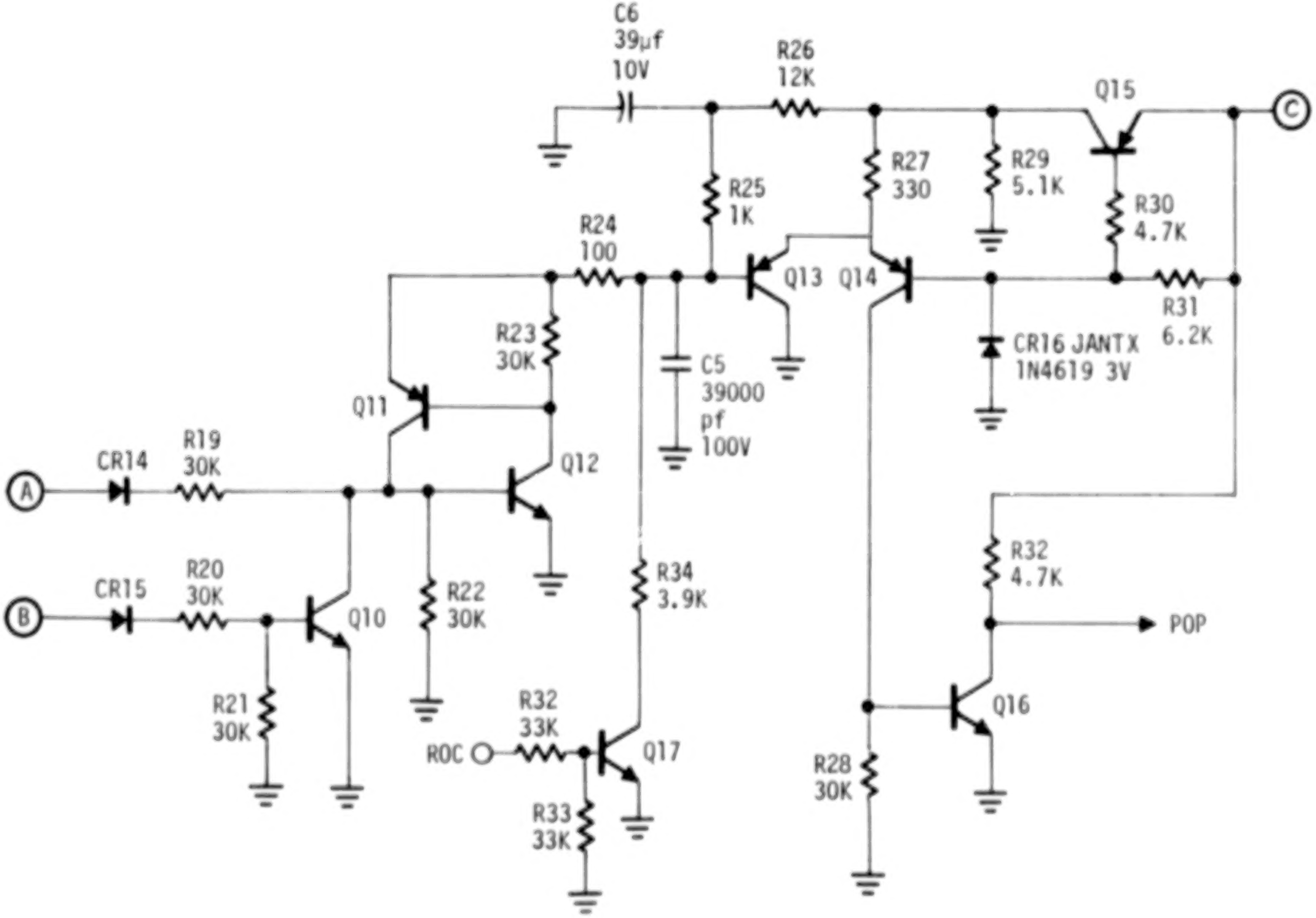
C6
39μf
10V
R26
12K
Q15
C
R27
330
R29
5.1K
R25
1K
R30
4.7K
R24
100
Q13
Q14
R31
6.2K
R23
30K
C5
39000
pf
100V
CR16 JANTX
1N4619 3V
Q11
CR14
R19
30K
A
Q12
CR15
R20
30K
B
Q10
R22
30K
R34
3.9K
R32
4.7K
POP
R21
30K
R32
33K
ROC
Q17
Q16
R28
30K
R33
33K

Figure 7-4. Pop Circuit

8.0 SSDR MECHANICAL DESIGN

8.1 GENERAL DESCRIPTION

The SSDR design as described in previous sections was physically packaged as illustrated in the photograph of Figure 8-1. The recorder has a volume of 860 in^3 and a fully populated weight of 47.2 pounds. In partitioning the packaging for the SSDR, the design is made up using four separate modules. On a functional basis, these modules include two memory modules, a drive and control unit module and a power supply module. As shown in Figure 8-2, these modules are vertically stacked and through bolted to form the total system package. A summary of the physical characteristics of the SSDR is given in the following table.

Table 8-1 - SSDR Physical Characteristics

Assembly	Qty.per System	Length in.	Width in.	Height in.	Volume in^3	Weight lb.
SSDR	1	12.75	12.70	5.20	858.6	47.2
Memory Module (MM)	2	12.75	12.70	1.40	226.8	13.8
Drive and Control Unit (DCU)	1	12.75	12.70	1.60	259.2	5.0
Power Supply Module (PSM)	1	12.75	12.70	.80	129.6	11.0
Miscellaneous	-	--	--	.10	16.2	3.6

The design storage capacity of 10^8 bits is equally divided between the two memory modules with each memory containing thirty-two memory cells each. The design population and memory allocation for the partially populated system is summarized in Table 8-2.

Table 8-2 SSDR Population

Storage Level	Fully Populated Quantity			Partially Populated Quantity		
	Chips	Carriers	Cells	Chips	Carriers	Cells
SSDR	1024	128	64	128	16	8
Memory Module 1	512	64	32	96	12	6
Memory Module 2	512	64	32	32	4	2

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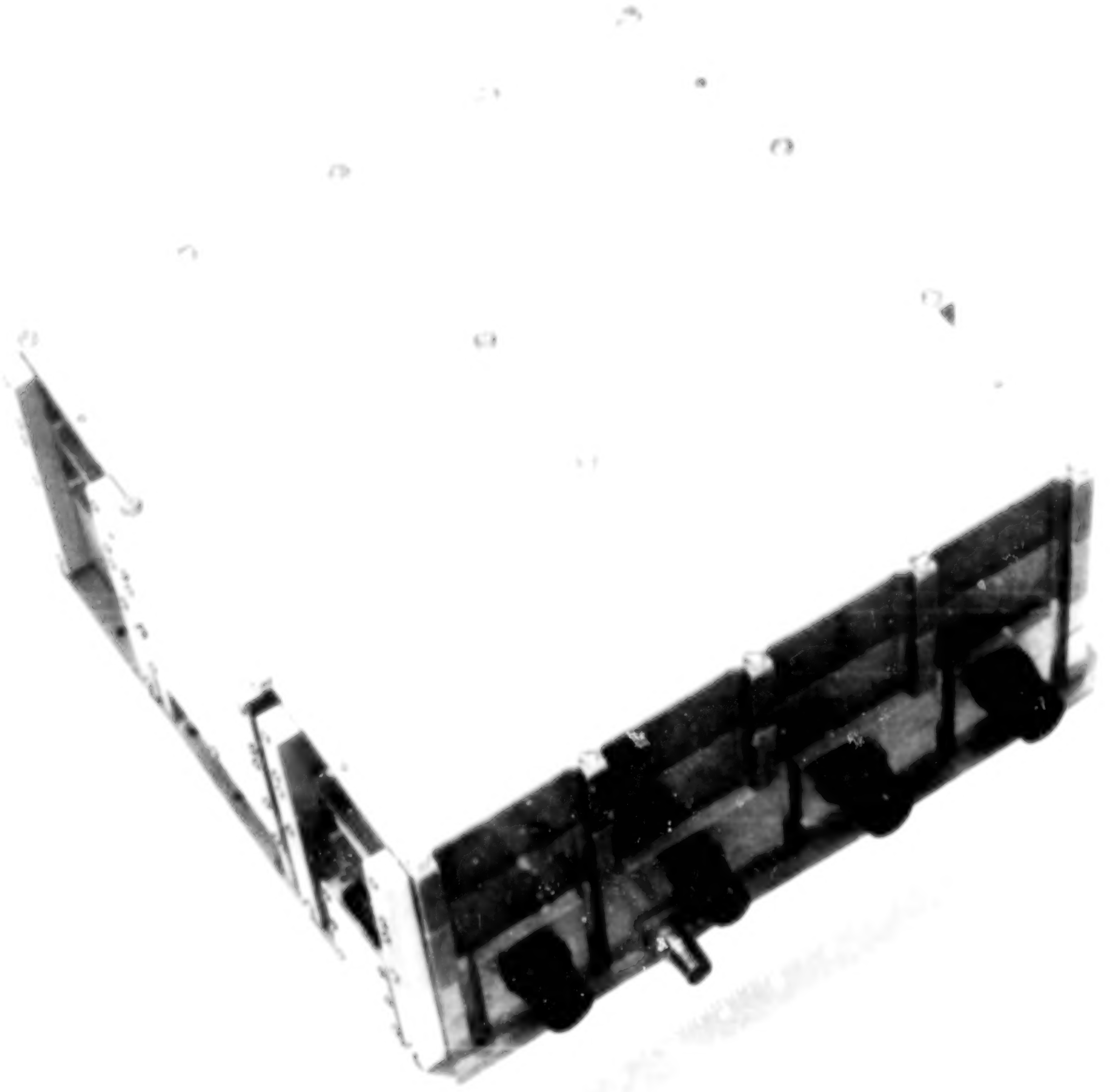

Fig 8-1. Solid State Data Recorder

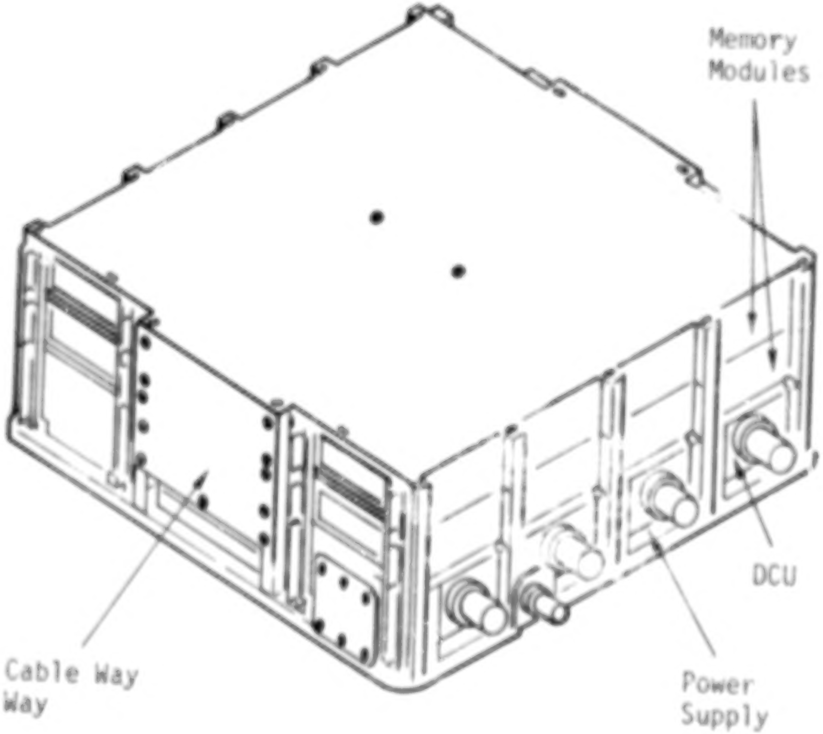
Memory
Modules
DCU
Power
Supply
Cable Way
Way

Figure 8-2. Solid State Spacecraft Data Recorder

8.2 SYSTEM MECHANICAL ASSEMBLY

The PSM is lowermost in the system assembly and serves as a mechanical and thermal interface for the system to spacecraft cold plate. As shown in Figure 8-2 and schematically in Figure 8-3 the Drive and Control Unit (DCU) and two Memory Modules (MM1, MM2) are stacked one above the other respectively with a top system cover. Sixteen high strength No. 8 throughbolts pass through holes in the upper modules and thread into inserts located in the power supply frame. The force produced by torquing these throughbolts serves to constrain the modules in the Z direction by compression and the X-Y direction by friction. The intermodule interfaces at the 14 perimeter throughbolt locations are under high pressure to produce a low thermal resistance for heat conduction.

A flange around the perimeter of the PSM frame is drilled in twenty places to accept No. 8 bolts which secure the system and produce a high pressure thermal interface to the spacecraft cold plate.

Other hardware associated with the system assembly include three cableway covers and eight 1100 alloy aluminum Z heat rail bars located as shown in Figure 8-3.

The electrical interface for the SSDR is via five Malco Mark 53 metal shell polarized circular connectors as shown in Figures 8-2 and 8-4. Four of these connectors are part of and interface with the DCU and the fifth (power) connector is part of and interfaces with the PSM.

The PSM is interconnected to the DCU using one Malco MCJM 48 pin metal shell connector set which is located behind the small cover located at the interface between the PSM and DCU.

As illustrated in Figure 8-4, each of the two MM's are interconnected to the DCU by three Malco MCJM 48 pin connector sets, the receptacles being located on one end of each MM. The mating plugs are hardwired to the DCU, these being located on either side of the SSDR behind the large access covers shown in Figure 8-2. The MM's are rotated 180° with respect to each other when assembled in the SSDR in order to allow mating of their respective connector sets.

8.3 MEMORY MODULE MECHANICAL DESIGN

The SSDR Memory Module as shown in Figure 8-5 has a design capacity of 5×10^7 bits, weighs 13.8 lb. and has a volume of 227 in^3. The MM is designed to structurally support and interconnect 32 cells to sense, operator and coil drive electronics. In addition the MM is also designed to have minimum weight and volume as well as provide efficient conduction paths for transfer of heat dissipated by various electronic and magnetic components. Physical location and modularity of functional subassemblies is dictated by logical grouping of components from a circuit standpoint and by the requirement to minimize noise

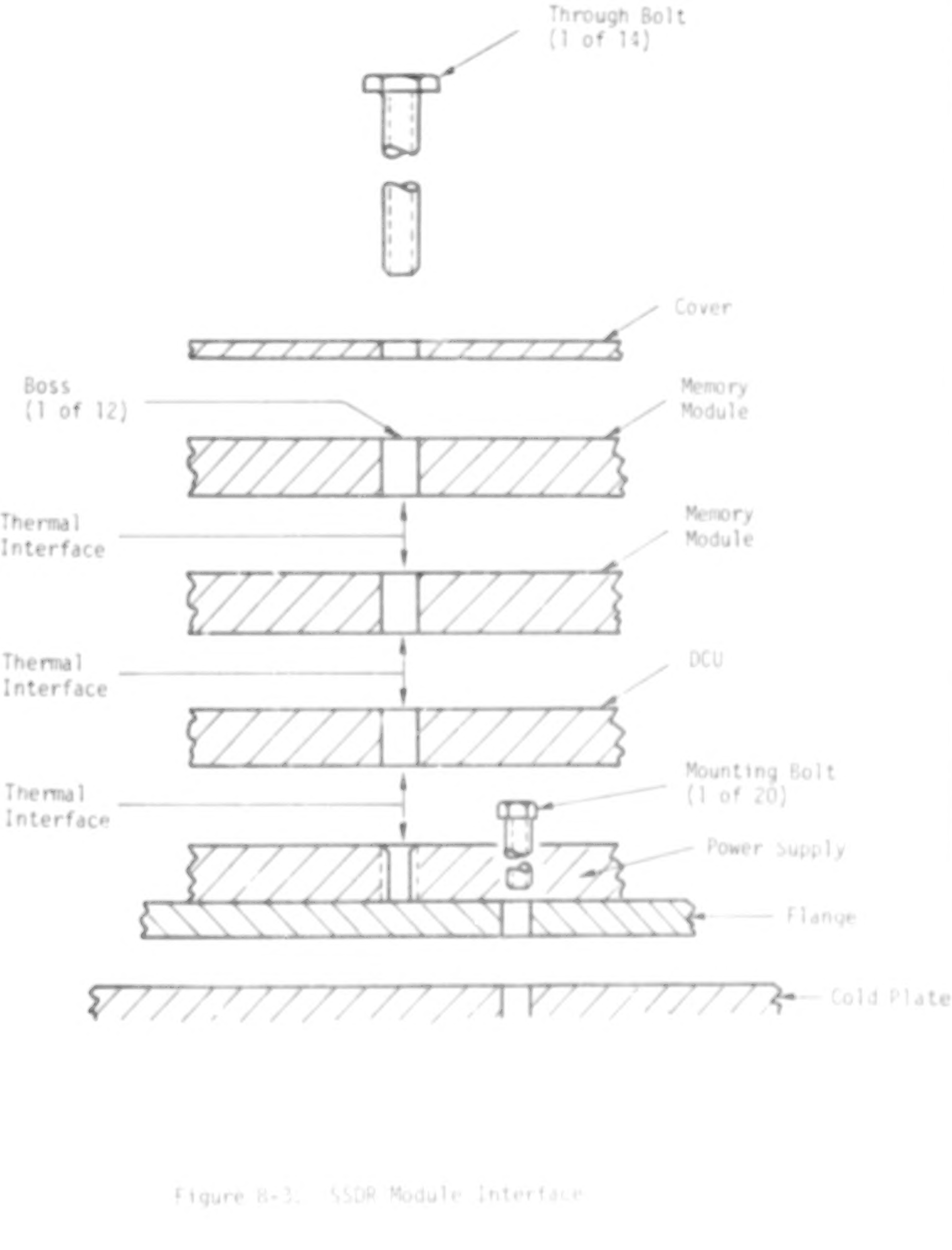
Through Bolt
(1 of 14)
Cover
Boss
(1 of 12)
Memory
Module
Thermal
Interface
Memory
Module
Thermal
Interface
DCU
Thermal
Interface
Mounting Bolt
(1 of 20)
Power Supply
Flange
Cold Plate

Figure 8-3. SSDR Module Interface

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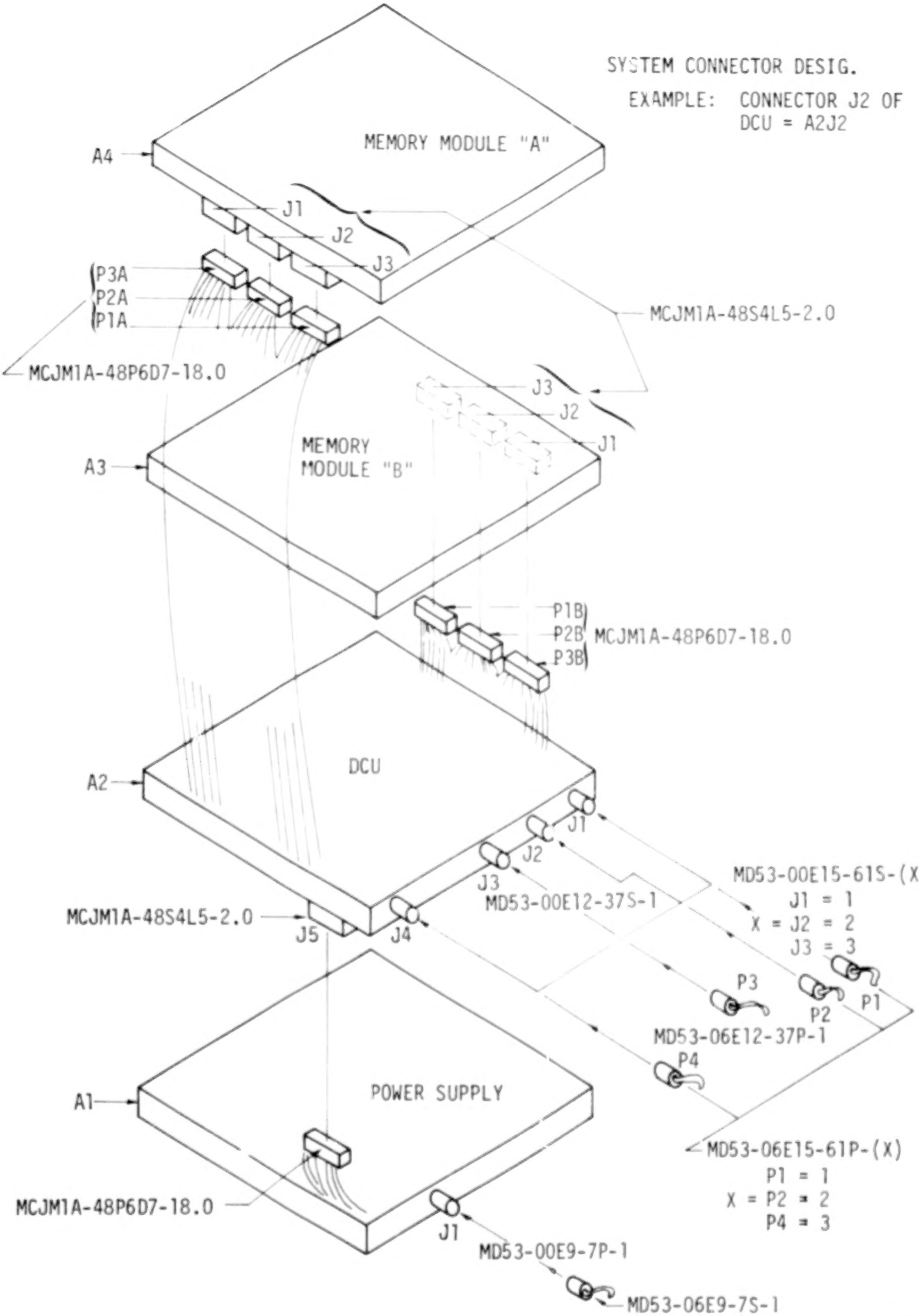
SYSTEM CONNECTOR DESIG.
EXAMPLE: CONNECTOR J2 OF DCU = A2J2
A4
MEMORY MODULE "A"
J1
J2
J3
P3A
P2A
P1A
MCJM1A-48S4L5-2.0
MCJM1A-48P6D7-18.0
J3
J2
J1
A3
MEMORY MODULE "B"
P1B
P2B
P3B
MCJM1A-48P6D7-18.0
A2
DCU
J1
J2
J3
MD53-00E15-61S-(X)
J1 = 1
X = J2 = 2
J3 = 3
MD53-00E12-37S-1
MCJM1A-48S4L5-2.0
J5
J4
P3
P2
P1
MD53-06E12-37P-1
P4
A1
POWER SUPPLY
MD53-06E15-61P-(X)
P1 = 1
X = P2 = 2
P4 = 3
MCJM1A-48P6D7-18.0
J1
MD53-00E9-7P-1
MD53-06E9-7S-1

Fig 8-4 - Solid State Data Recorder System/Connector Ref. Designations

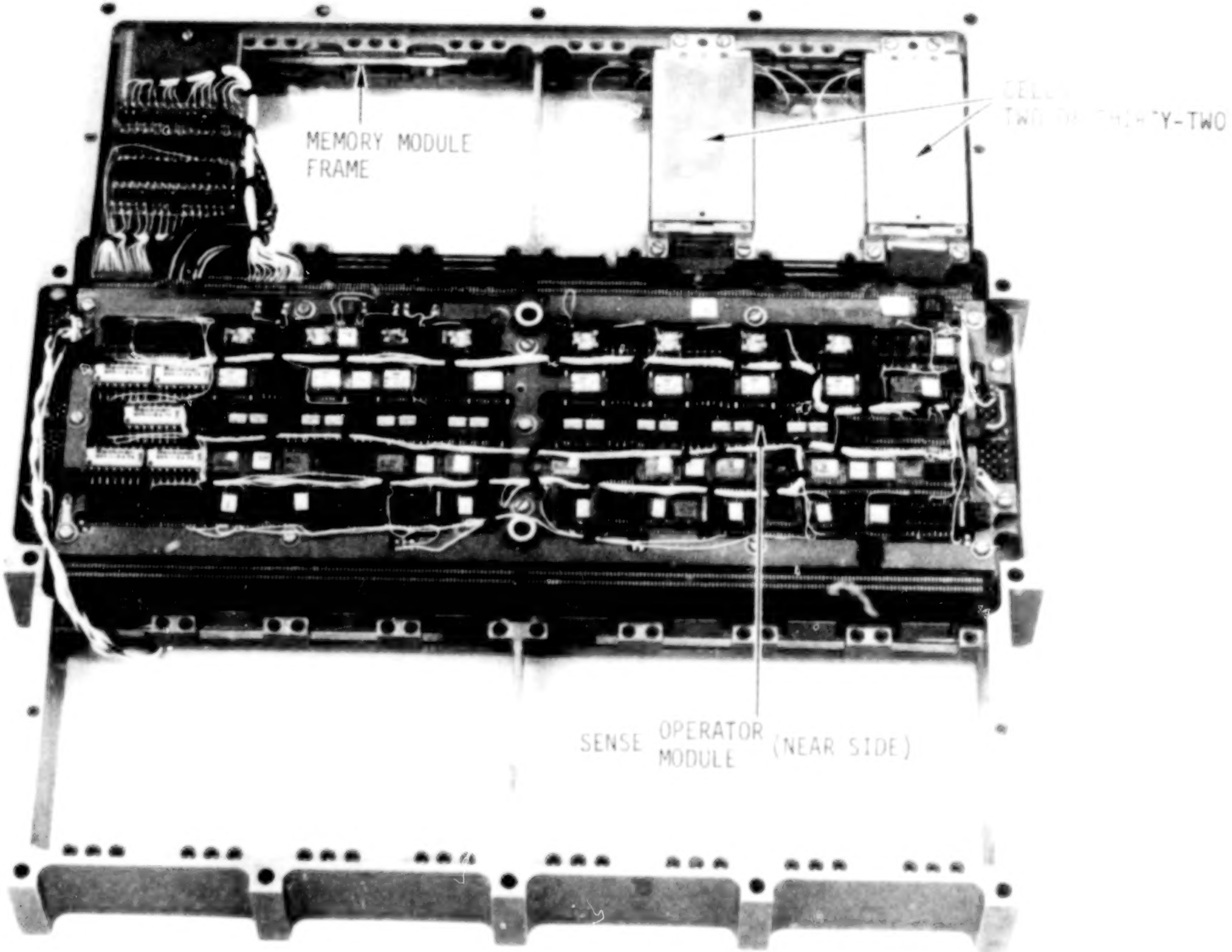
MEMORY MODULE FRAME
CELLS
TWO OF THIRTY-TWO
SENSE OPERATOR MODULE (NEAR SIDE)

Fig 8-5. SSDR Memory Module

in the sense channels. A design consideration with respect to noise is illustrated by the requirement that the coil driver circuits operate at 65 volts and 3 amps whereas bubble signals of 4 to 8 millivolts must be matrixed for 32 cells and detected. Details of the SSDR MM design implemented are described in the following paragraphs.

Principal components of the MM include 32 cells, a sense operator module (SOM), coil driver module (CDM), balun/diode modules, frame, interconnect and cooling components. As shown in Figure 8-6, the cells are organized into two groups of 16; each group having all of their carrier flexible cables terminate at the SOM. The CDM is located beneath the SOM and is hard wired to each of the cells via 16 balun/diode modules (BDM) used to implement the coil drive matrix.

An aluminum frame is used to provide mounting for the thirty-two memory cells and two MLB's. The cells are divided into two groups of sixteen mounted along two opposite edges of the memory module. Cells are mounted in pairs, one above the other, along these ec . This mounting is illustrated in Figure 8-7. Each lower cell has a balun/diode module (BDM) adhesively bonded to the exposed bias shell surface. Cabling (not shown) from the coil drive MLB terminates to the inboard side of the BDM with X, Y and Z coil leads from the cell connected to the outboard side of the BDM. Sense and operator lines are connected between cell and sense operator module via flex cables and transition strips. The transition strips are soldered to the sense/op MLB and bonded in place prior to assembly. The flex cable is soldered and bonded to the cell prior to assembly. Connection of the flex circuit and transition strips is made during final assembly in the memory module.

Interconnection of the memory module to the DCU is made by three Malco MCJM connectors mounted at one end of the memory module (see Figure 8-4). The relative position of the two memory modules in the system are interchangeable by simply rotating the two modules 180°. The address designation of a memory module is established by its physical location in the system.

A summary of memory module physical characteristics is given in Table 8-3 below.

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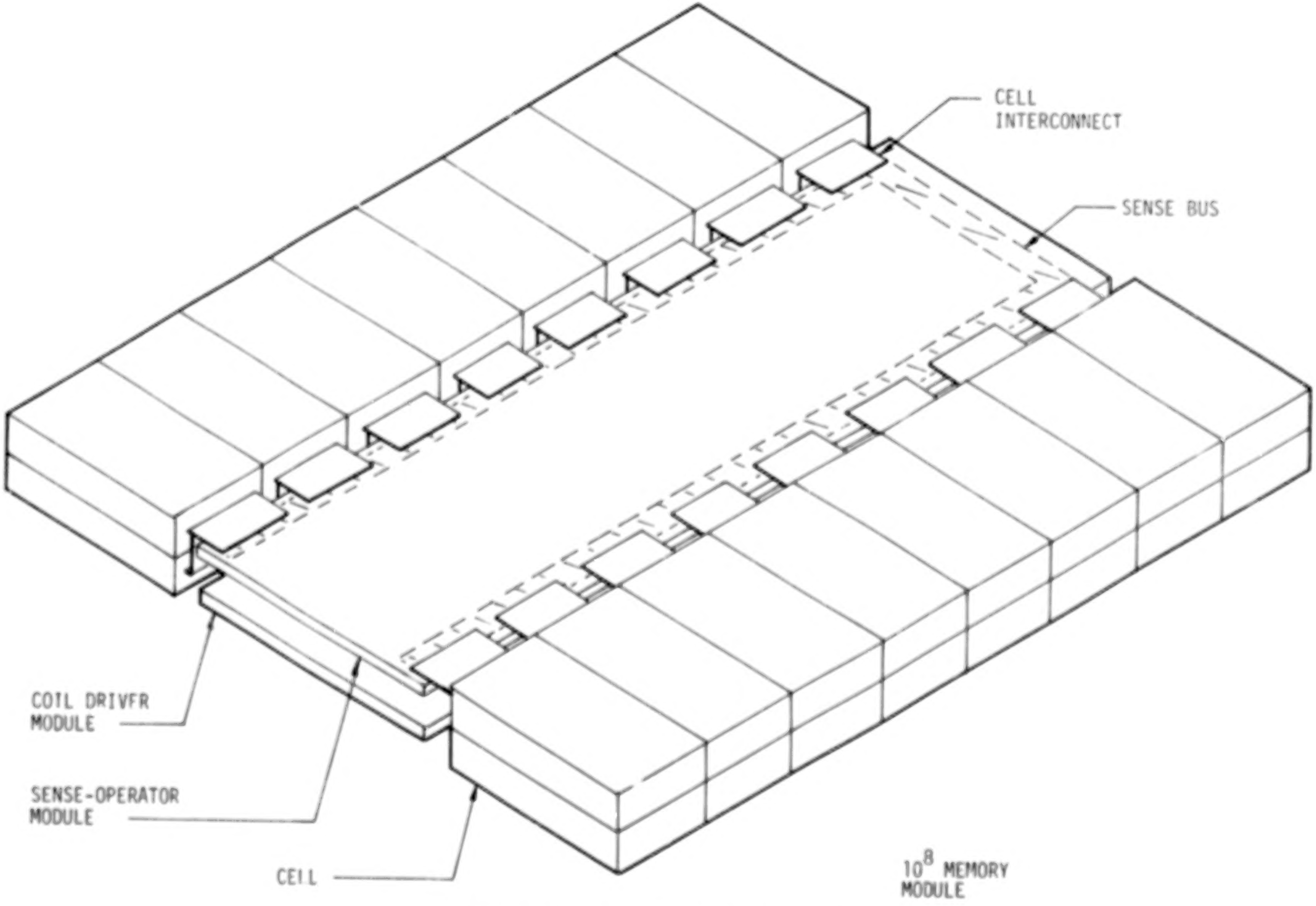
CELL
INTERCONNECT
SENSE BUS
COIL DRIVER
MODULE
SENSE-OPERATOR
MODULE
CELL
10^8 MEMORY
MODULE

FIGURE 8-6. MEMORY MODULE CONFIGURATION

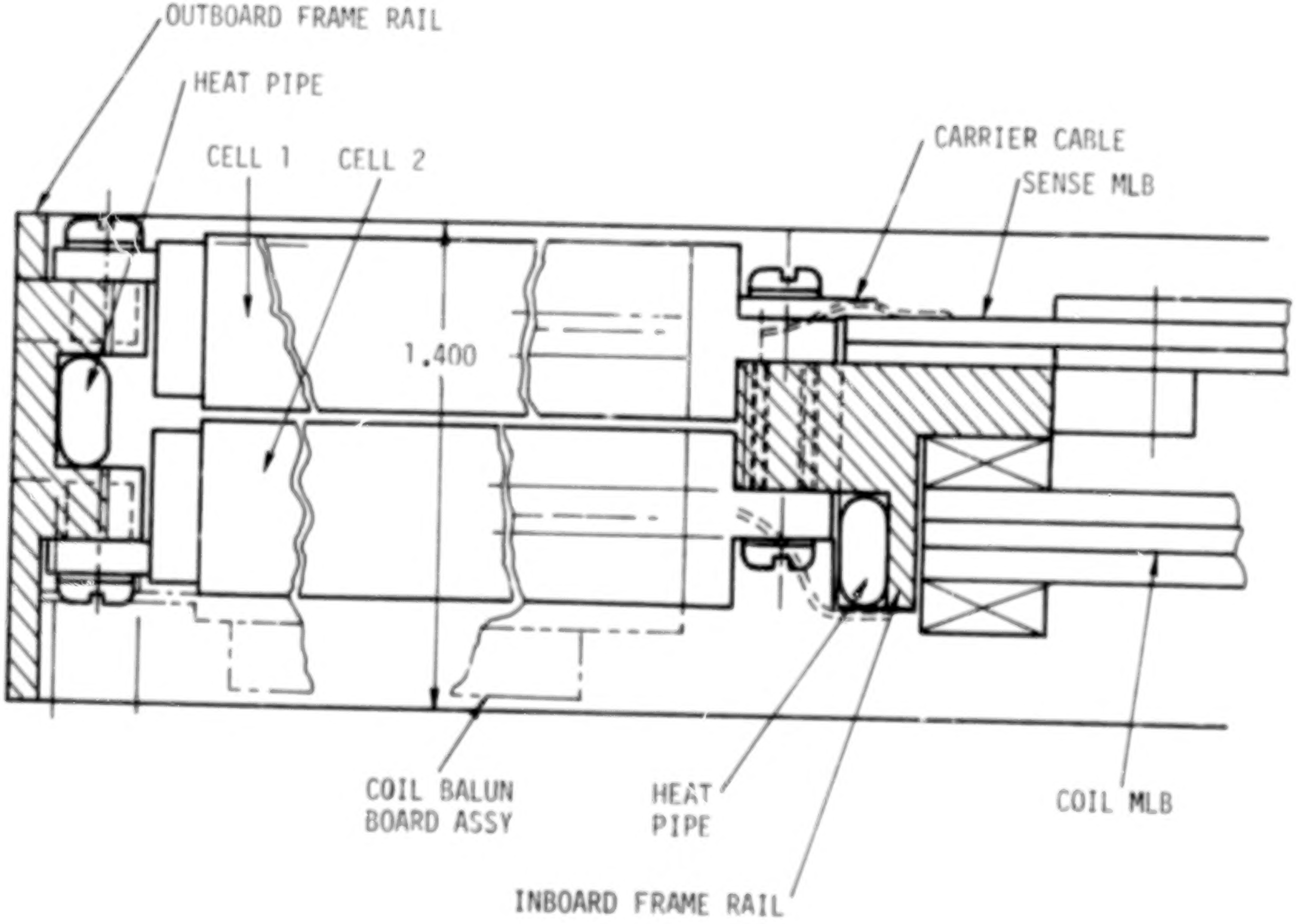
OUTBOARD FRAME RAIL
HEAT PIPE
CELL 1
CELL 2
CARRIER CABLE
SENSE MLB
1.400
COIL BALUN BOARD ASSY
HEAT PIPE
COIL MLB
INBOARD FRAME RAIL

FIGURE 8-7. CELL MOUNTING DETAIL

Table 8-3 Memory Module Physical Characteristics

Assembly	Qty Per MM	Length in.	Width in.	Height in.	Volume in^3	Weight lb.
Memory Module (MM)	1	12.75	12.70	1.40	226.8	13.8
Cell	32	2.95	1.48	.51	71.4(32)	8.9(32)
Sense Operator Module (SOM)	1	12.40	5.30	.55	36.1	1.0
Coil Driver Module (CDM)	1	12.40	4.80	.75	44.6	1.2
Balun/Diode Module (BDM)	16	2.95	1.40	.27	17.8(16)	.6(16)
Frame	1	12.75	12.70	1.40	226.8	2.1

8.3.1 Sense Operator Module

The Sense Operator Module (SOM) terminates and interconnects 32 cells into a component array having sense and operator electronic circuit functions. Input-output to the MM and coil driver module (CDM) are also provided on the SOM.

Primary design guidelines for the SOM require maximum density component placement, minimum component height, uniform sense matrix layout geometry with maximum isolation of signal traces from power and logic traces. Physical characteristics of the SOM are given in Table 8-3.

Principle components of the SOM include a ten layer 0.100-inch thick multilayer PWB (MLB), 1100 alloy aluminum heat rail panels, approximately 440 integrated and discrete electronic components, I-O connectors and interconnect/transition flexible cables.

As previously noted a transition cable assembly is required in order to facilitate termination of the carrier flexible cables which have conductors on 25 mil centers. The transition cable fans out to 50 mil centers at the MLB end and is lap soldered via integral extended beam leads which are part of the cable. The transition cables are adhesively bonded and terminated to both sides of the MLB and permit the bottom cell flexible cables to be terminated after the SOM is secured to the MM.

8.3.2 Coil Drive Module

The Coil Drive Module as shown in the photograph of Figure 8-8 provides the circuitry to generate the rotating field in the X and Y coils of the memory cells. A six layer MLB is used to implement the coil drive function. Significant weight and volume savings are achieved through the use of twenty-five hybridized coil drive voltage switches that are used in place of the 244 discrete components that would be required to implement this function. Each of the 42 pin hybrid packages contains two coil drive switches. In addition to the hybrids, the coil drive MLB contains 269 discrete components and 24 drive transformers.

8.3.3 Balun/Diode Modules

Balun/diode modules (BDMs) are adhesively bonded to each of 16 cells. Each of the BDM's have four balun transformers and 16 diodes which are adhesively bonded and lap solder terminated to a two sided PWB .008 inch thick. The PWB is adhesively bonded to a .025 inch thick 1100 alloy aluminum plate which is thermally terminated at the outboard cell mounting interface. Heat dissipated by the diodes is conducted through the diode leads to the aluminum plate by heavy wall plated through holes and through a thin polyimide/adhesive interface. As previously discussed each BDM terminates the coil wiring from two cells and the required lines from the CDM harness.

8.3.4 Frame

The SSDR memory module frame mechanically and thermally integrates the various functional assemblies into a composite assembly capable of surviving the imposed environments with a positive margin of safety. The frame is machined from 6061-T6 alloy aluminum plate, stress relieved and provided with self locking cres inserts at all threaded fastener positions. Heat dissipated by various sources within the MM is transferred and distributed by heat pipes which are adhesively bonded into machined slots using a high conductivity aluminum oxide filled epoxy resin.

8.4 DRIVE AND CONTROL UNIT

The DCU module,as shown in Figure 8-9, controls most functions within the SSDR and contains four microprocessors, 500 integrated circuits, a RAM core memory and two PROM's on a twelve layer MLB Both memory modules are interconnected to the DCU via stranded wire cables which are wired to the DCU MLB. In addition, the DCU contains all I/O interconnects. The DCU is housed in a 6016-T6 machined and stress relieved aluminum frame, which provides the clearance necessary to accomodate various power supply components mounted below. All circuitry for the DCU is carried in a single 1 ft^2 MLB and heat transfer is via surface heat rails as in the memory modules. The DCU weighs 5.0 lb. and has a volume of 269 in^3.

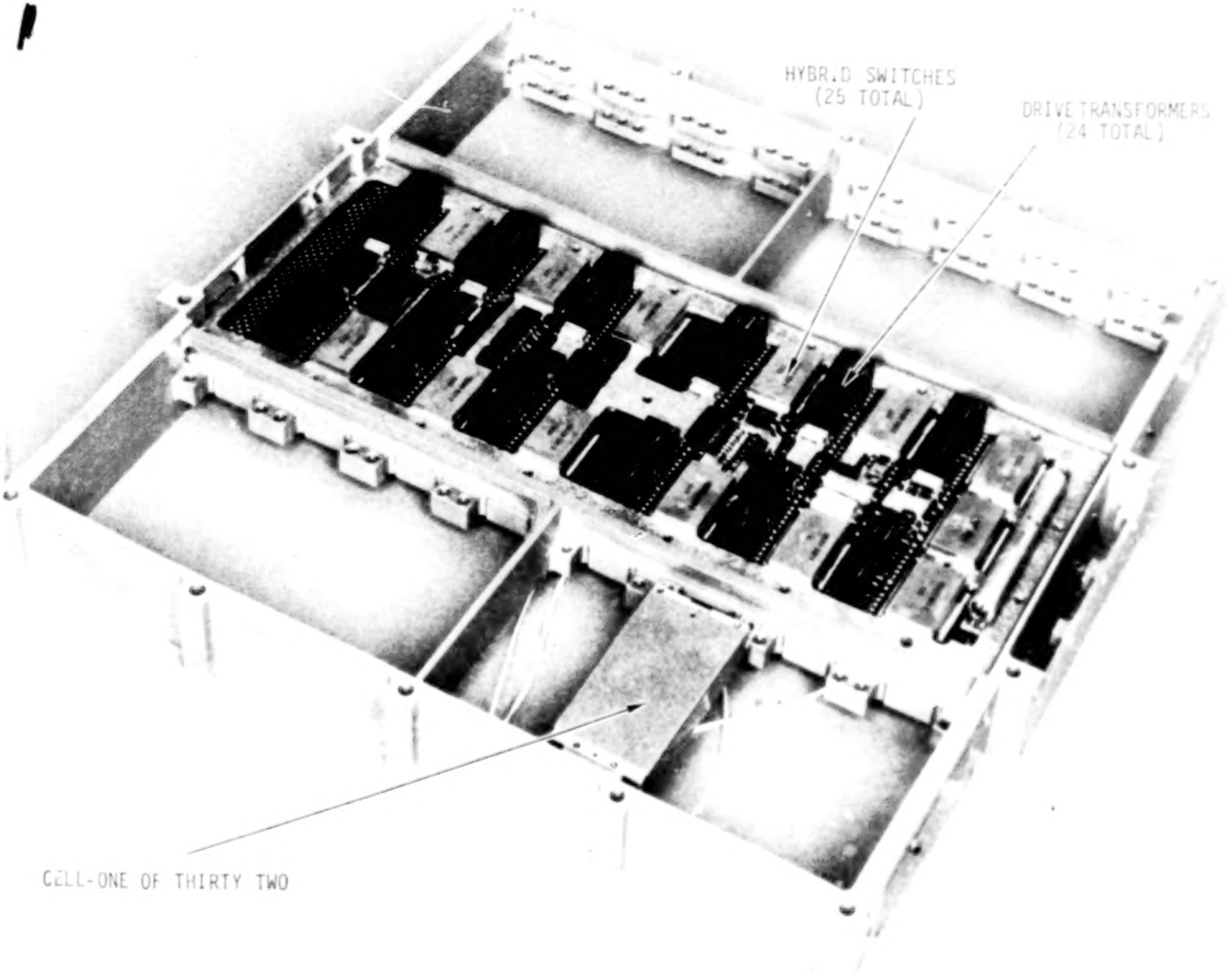
HYBRID SWITCHES
(25 TOTAL)
DRIVE TRANSFORMERS
(24 TOTAL)
CELL-ONE OF THIRTY TWO

Fig 8-8. Coil Drive Module

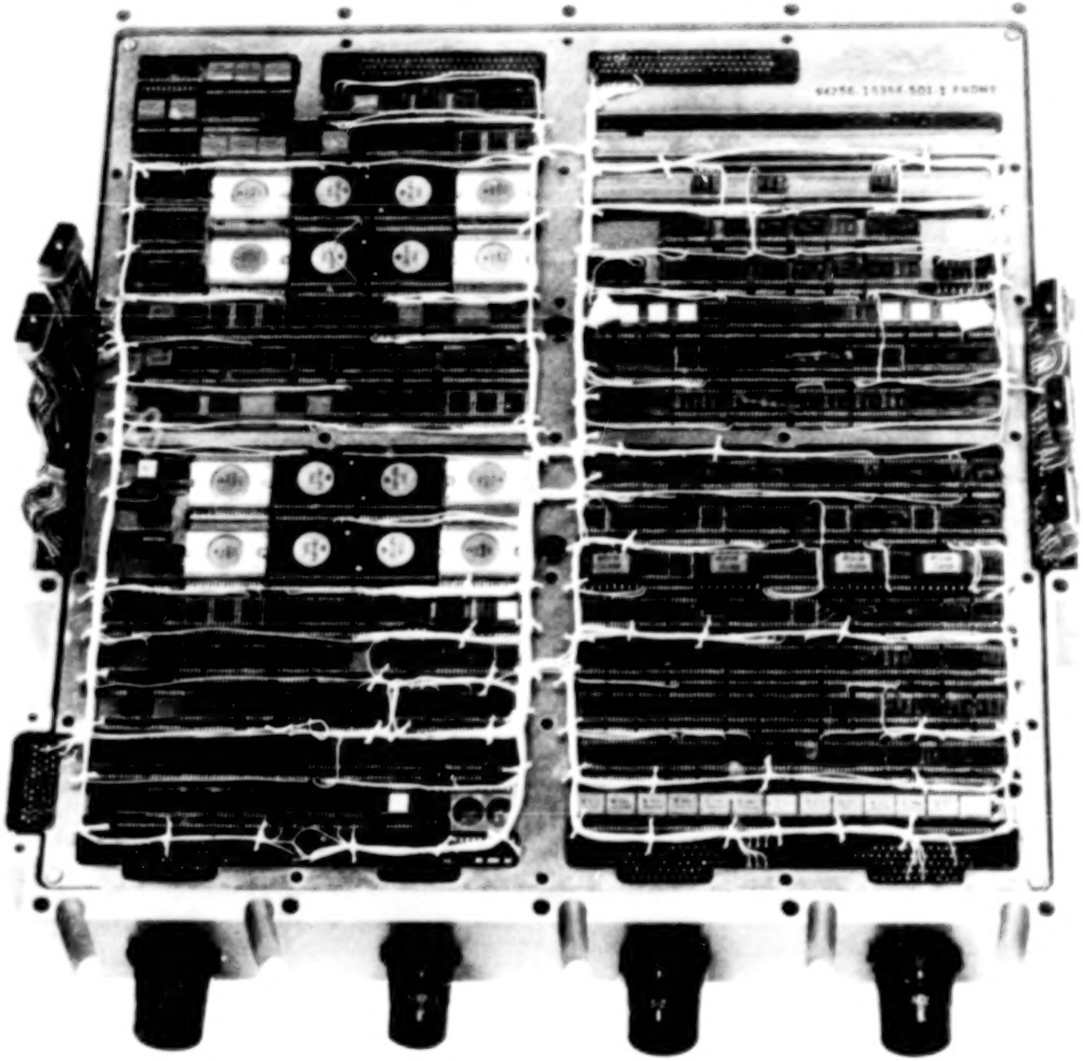

Fig 3-9. Drive and Control Unit

8.5 POWER SUPPLY MODULE

The Power Supply Module (PSM), as shown in Figure 8-10, is the structural base for the SSDR and provides the mechanical and thermal interface from the SSDR to the spacecraft cold plate. The PSM weighs 11.0 lb. and has a volume of 130 in^3.

The PSM frame is a low rectangular box milled from 6061-T6 aluminum plate and stress relieved. A central main rib and intersecting cross rib carry dynamic loads from the center system throughbolts and modular components to the frame perimeter. Commercially available modular power supply components provide the power conversion and are secured to the .125 thick bottom wall of the frame by threaded fasteners and thermally conductive adhesive. High dissipation modular supplies are mounted around the inner perimeter of the frame in close proximity to a mounting flange which is machined into the PSM frame outer perimeter. Twenty holes are drilled into the flange to accept No. 8 screws required to secure the SSDR to the cold plate and provide the force necessary to produce a low thermal resistance interface.

Other components of the PSM include a power control module, filtered feedthroughs and input-output connectors previously discussed. Electro static shielding is provided by a .025 thick aluminum cover (not shown).

8.6 MATERIALS

Material selection for the SSDR is divided into three physical categories these being polymeric, metallic and ceramic. Polymeric materials are selected wherever possible to meet without preconditioning total weight loss (TWL) and volatile condensable material (VCM) requirements for spacecraft environments and be capable of withstanding long term aging at 125°C. All materials are selected on the basis of suitability for the intended detail application. Thermal conductivity to weight ratios, strength to weight ratios and cost effectiveness criteria are major parameters influencing material selection when applicable.

8.6.1 Polymeric Materials

The principle guide to polymeric material selection with respect to acceptable thermal vacuum properties is the "JSC 08962 compilation of VCM data of non-metallic materials". Other sources include Autonetics Material and Process Laboratory Test Reports and Materials Specifications. Data is also supplied from other Rockwell programs involving the development of equipment for spacecraft environments.

Three additional selection criteria are used to measure the acceptability of a polymeric material for a particular detail application with respect to thermal vacuum. These criteria are as follows:

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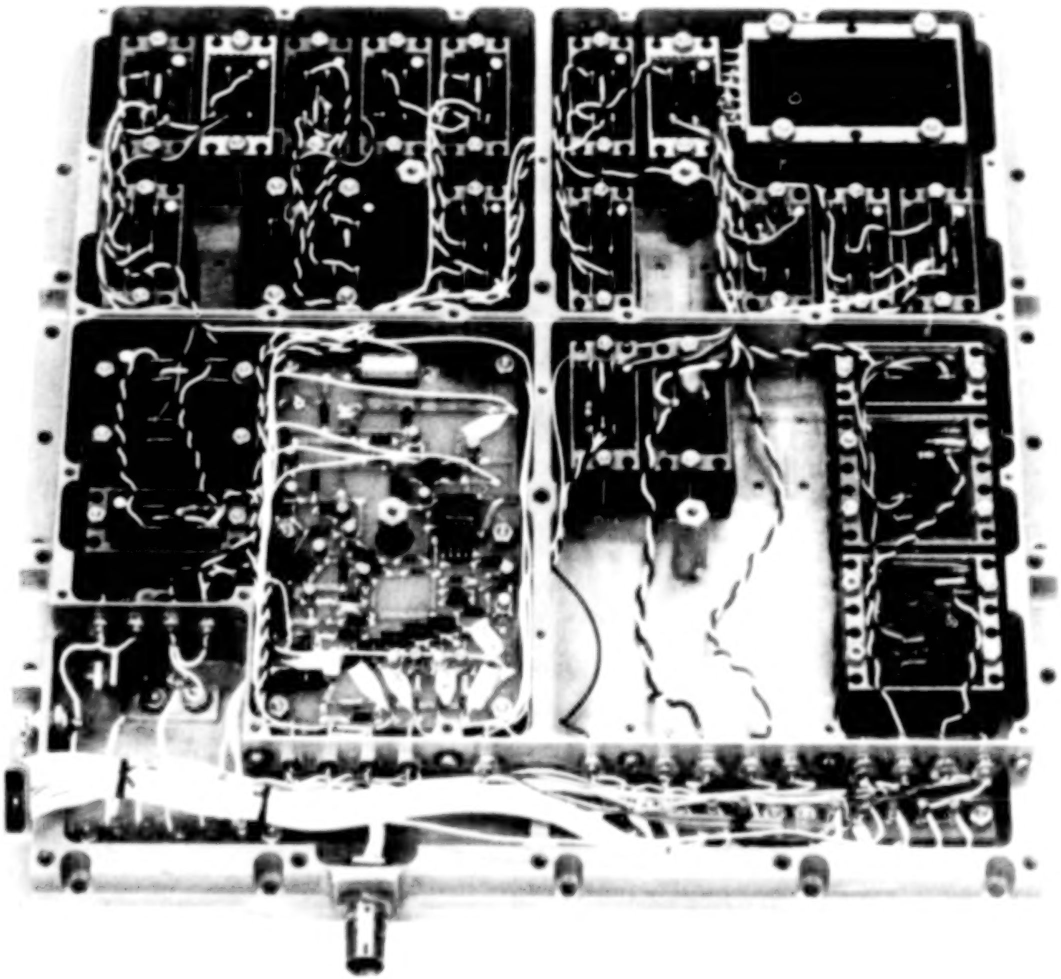

Fig 8-10. Power Supply Module

A. Material has acceptable thermal vacuum properties without preconditioning.

B. Material requires preconditioning in order to have acceptable thermal vacuum properties.

C. Material is acceptable only on the basis of expected qualification in assembly wherein only very small area of material is exposed to the thermal vacuum environment.

8.6.2 Metallic Materials

Principal parameters for selection of metallic materials are suitability for intended use, cost effectiveness and optimum thermal conductivity and/or strength to weight ratios (efficiency). The latter criteria are in some cases incompatible with satisfying both minimum weight and volume system requirements. In this case minimum weight criteria is used and the volume efficiency sacrificed. Exceptions to this criteria are also made when the gross weight of material required is small in comparison to system weight and thermal, strength or cost parameters favor the selection. Most materials considered are suitable for the specified environments with minimal additional surface protection.

Table 8-4 Metallic Material Properties

Material	Thermal Conductivity Watt/In-C°	Yield Strength 10^3 PSI	Density Lb/in^3	Conductivity To Weight Ratio	Strength To Weight Ratio
Copper	9.9	45	.323	30.6	139
Aluminum 6061	4.35	40	.098	44.4	408
Aluminum 1100	5.62	17	.098	57.3	173
Magnesium AZ31B	1.93	25	.064	30.1	390
Titanium T16AL	.18	130	.160	1.1	812
Beryllium	3.82	60	.067	57.0	895
Permalloy	.88	22	.316	2.8	69

8.6.3 Ceramic Materials

Ceramic materials are selected primarily on their suitability for intended use. Aluminum oxide is used for the bubble chip carrier thick film PWB substrate as it is the principal material commonly used in this process and compatible with design electrical and mechanical requirements.

Beryllium oxide is used because of its high thermal conductivity and insulating properties as required in its application to the SSDR bubble chip carriers and the CDM hybrids. In the hybrid application beryllium oxide is also compatible with refractory metallization processes.

9.0 MEMORY CELL TEST RESULTS

9.1 INTRODUCTION

During the SSDR program, eight memory cells were fabricated, tested and integrated into the two Memory Modules. This section describes the testing and data associated with these eight cells. Cell test equipment, memory element matching, test sequences and test flow are discussed.

9.2 MEMORY CELL POPULATION AND TEST

The general process flow used for population and test of the memory cells is illustrated by the chart of Figure 9-1. Basically there are three primary objectives of this series of tests. First is to determine by wafer level test which chips have required operating margins and to characterize each acceptable device in terms of its operating bias range. Test at this level is done by a programmed sequencing wafer prober. Test criteria at this level are based on characteristic sensitivities of the memory element and are designed to achieve a reasonable confidence in device operation with a minimum investment in test time. These tests are run in a start-stop mode using a worst case sixteen bit data pattern consisting of 1111111001011000. Operator and drive field are fixed for this test with bias field being the test variable. Figure 9-2 is a flow chart of the wafer test sequence.

After wafer test, the wafer was scribed and broken and the good die identified and stored. The optional die level test using the wafer prober is included only as a trouble shooting aid for problems in the scribing and breaking process. After solving some initial problems with this process early in the program, this test step was not used. The second objective of this test sequence is selection of the sixteen die that are to be grouped in a single memory cell. The basic criteria in selection of chips is to match the operating bias fields of the sixteen memory elements such that the composite bias margin of the cell is adequate. Selection criteria used on the SSDR cells required a composite bias margin of 6 oe at 25°C. Additional requirements were that the collapse field of all devices match within a 3 oe band and that the q of the devices be equal to within ± 1. These two parameters are material characteristics measured on the wafer from which the elements are fabricated. Using material parameters gives additional confidence that element characteristics not only match at a given temperature but will match over a temperature range having a uniform temperature coefficient that also matches the coefficient of the bias magnets.

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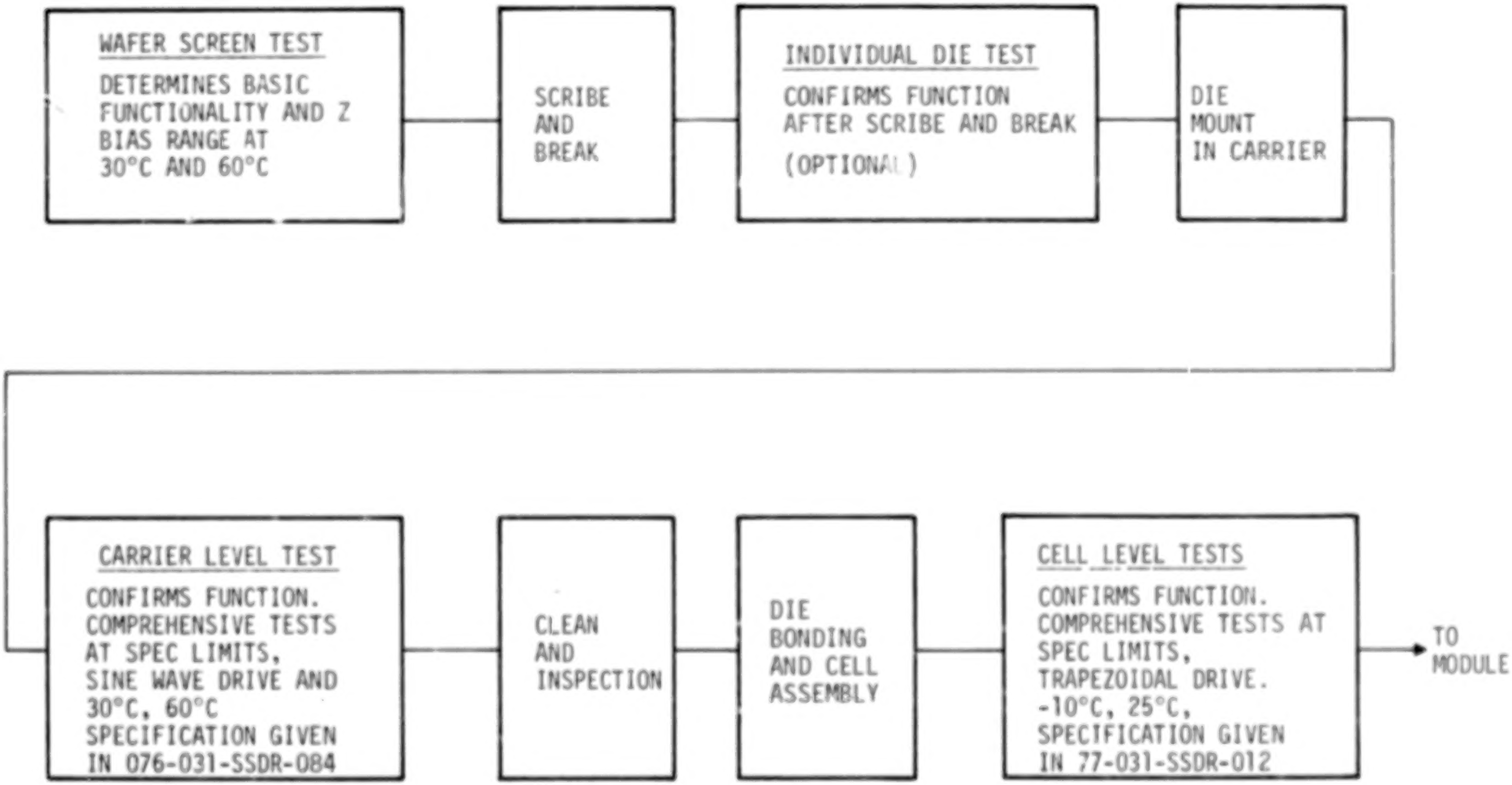
WAFER SCREEN TEST
DETERMINES BASIC FUNCTIONALITY AND Z BIAS RANGE AT 30°C AND 60°C
SCRIBE AND BREAK
INDIVIDUAL DIE TEST
CONFIRMS FUNCTION AFTER SCRIBE AND BREAK
(OPTIONAL)
DIE MOUNT IN CARRIER
CARRIER LEVEL TEST
CONFIRMS FUNCTION. COMPREHENSIVE TESTS AT SPEC LIMITS, SINE WAVE DRIVE AND 30°C, 60°C SPECIFICATION GIVEN IN 076-031-SSDR-084
CLEAN AND INSPECTION
DIE BONDING AND CELL ASSEMBLY
CELL LEVEL TESTS
CONFIRMS FUNCTION. COMPREHENSIVE TESTS AT SPEC LIMITS, TRAPEZOIDAL DRIVE. -10°C, 25°C, SPECIFICATION GIVEN IN 77-031-SSDR-012
TO MODULE

Figure 9-1. Cell Test Sequence

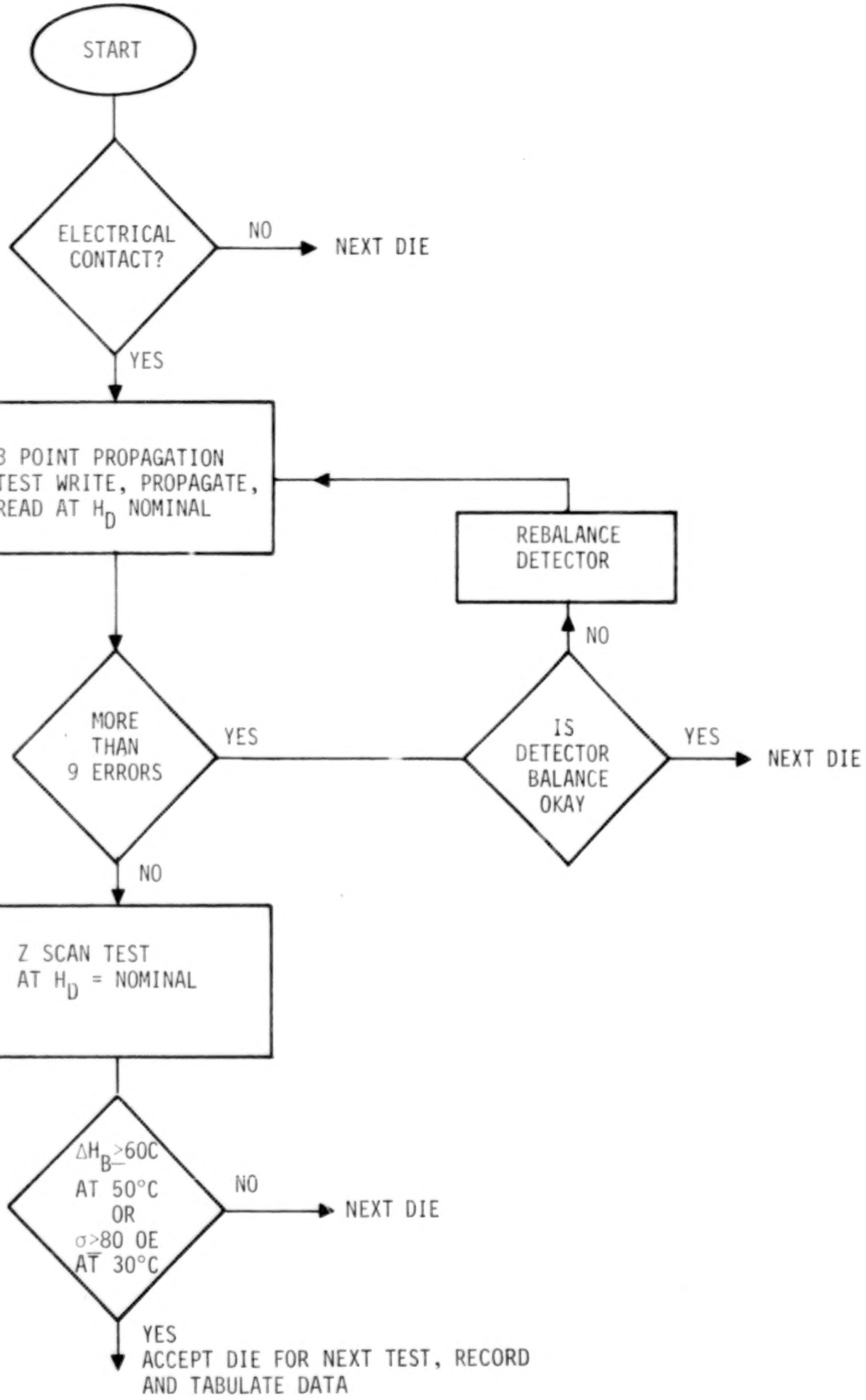
START
ELECTRICAL CONTACT?
NO
NEXT DIE
YES
3 POINT PROPAGATION TEST WRITE, PROPAGATE, READ AT H_D NOMINAL
REBALANCE DETECTOR
NO
MORE THAN 9 ERRORS
YES
IS DETECTOR BALANCE OKAY
YES
NEXT DIE
NO
Z SCAN TEST AT H_D = NOMINAL
$\Delta H_B \geq 60C$ AT 50°C OR $\sigma > 80$ OE AT 30°C
NO
NEXT DIE
YES
ACCEPT DIE FOR NEXT TEST, RECORD AND TABULATE DATA

Figure 9-2. Wafer Screen Test

After sixteen chips have been selected for populating a cell, they are mounted on the two memory cell substrates. Prior to lead bonding, the mounted chips are confidence tested using the wafer probe test equipment. After all chips operate satisfactorily, lead bonds are made between memory element and substrate and the substrates are installed into a cell with bias field adjusted to the center value for the sixteen chips. At this point, the cell enters the third and final phase of the sequence which is a comprehensive cell test. This test was designed to be a true worst case test of cell operation exercising all relevant cell operating variables. A cell test system was designed which tested the cell using coil drive and sense circuitry identical to that used in the Memory Module. Drive function amplitudes and timing, sense threshold and cell temperature could be varied during test. The general test philosophy used on the cell is illustrated in Figure 9-3. A maximum deviation from nominal bias setting was established from a worst case analysis as +1 oe and -1.5 oe. By using the Z coil built into the cell, this bias field was perturbed by these amounts and tested at both high and low drive field limits as indicated by Points 1, 2, 3 and 4 in Figure 9-3. This test sequence was run at room temperature, -10°C and 60°C. Generate and annihilate function amplitude was set at worst case conditions for the particular test conditions being run. Tests were also run to establish that the cell meets maximum no bubble signal and minimum bubble signal requirement.

9.3 MEMORY CELL TEST RESULTS

A significant amount of data was obtained from the detailed test of the eight cells which resulted in identification of a number of problems. These problems were basically temperature related problems and detector problems. Major temperature problems were a low end drive field limitation at -10°C and (H_{Min} >50 oe) bias field margin overlap problems at 60°C. On a statistical basis these problems occurred often enough that it was judged to be impractical to fabricate the number of devices that would be required to obtain matched sets of memory elements that would meet the original operating temperature goal. Because of this, a decision was made to reduce the required temperature range to 0°C to 50°C. Cell test procedures were modified to reflect this and SSDR cells were tested to this requirement.

The second major problem resulted from detector characteristics of the memory element. As a statistically significant number of elements were tested, it became clear that insufficient sense margin existed to operate the cells as planned using multiplexed sense amplifiers. Such an approach requires that chips at the same location in all cells have overlapping sense windows. Considering detector characteristics, cell noise and system noise, it was found that such a common threshold was not practically obtainable. A summary of sense related cell parameters is given in Table 9-1. In terms of chip related sensitivities, primary problem areas were a high and variable zero or no bubble signal resulting from dynamic mismatch between active and dummy detector and a bubble overlap signal resulting from fringing of adjacent bubbles into the detector. These two factors alone can generate a variable sense window degradation that is roughly half of the detector output

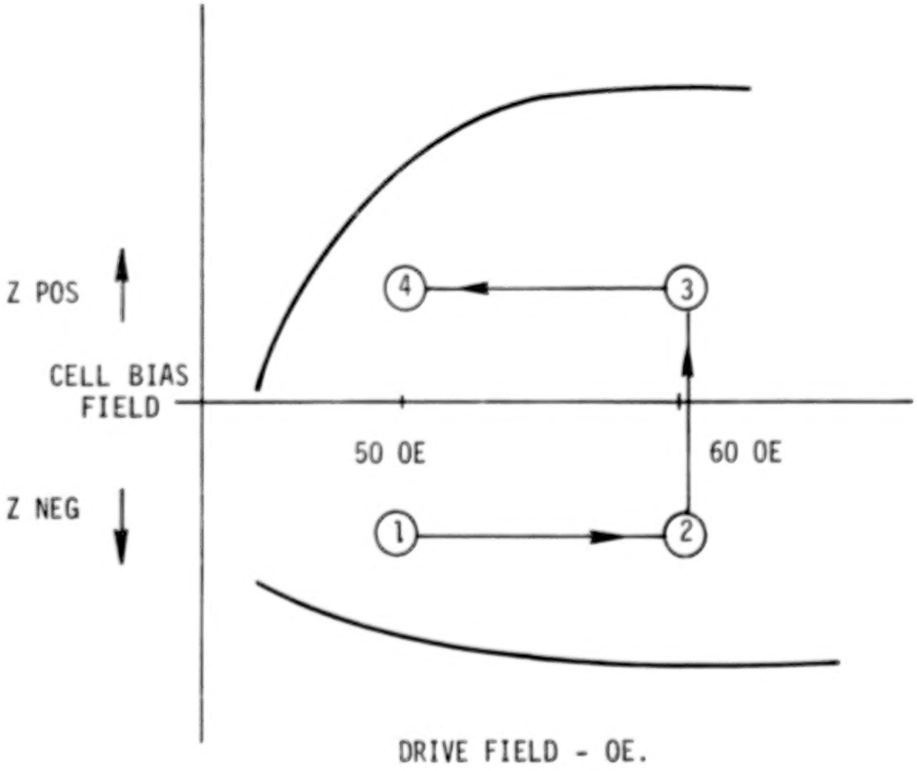
Z POS
CELL BIAS FIELD
Z NEG
50 OE
60 OE
①
②
③
④
DRIVE FIELD - OE.

Figure 9-3. Cell Test Philosophy

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PAGE

TABLE 9-1. BUBBLE SENSING STATISTICS

	ITEM	DEFINITION	VALUE		UNITS
			$\bar{X}$	σ	
CHIP RELATED	BUBBLE SIGNAL	THE BUBBLE INFLUENCE ONLY; "1" - "0" FOR A SINGLE BUBBLE AT 6 MA	.83	.25	MV/MA
	THERMAL COEFFICIENT "1 - 0"	A "1" - "0" FROM 25 C TO 50 C	-.33	--	%/°C
	ZERO SIGNAL	NO BUBBLE SIGNAL	+.03	.11	MV/MA
	"0" SIGNAL THERMAL COEFFICIENT	MEASURED AT 50 C RELATIVE TO 25 C	+.1	--	%/°C
	ADJACENT BUBBLE	ZERO COMPARED TO THE ZERO WITH AN EARLIER AND A LATE BUBBLE	±.12	.06	MV/MA
	DRIVE FIELD SENSITIVITY	CHANGE MEASURED IN SIGNAL AMPL INGOING FROM 50 - 60 OE	-.07	.03	$\frac{MV/MA}{10\ OE}$
CELL RELATED	CROSS COUPLED NOISE	DIFFERENTIAL NOISE FROM COIL TO SENSE LINES	±.31	.6	MV
	DØ/DT	VOLTAGE PICKUP FROM FIELD	±.15	.2	MV

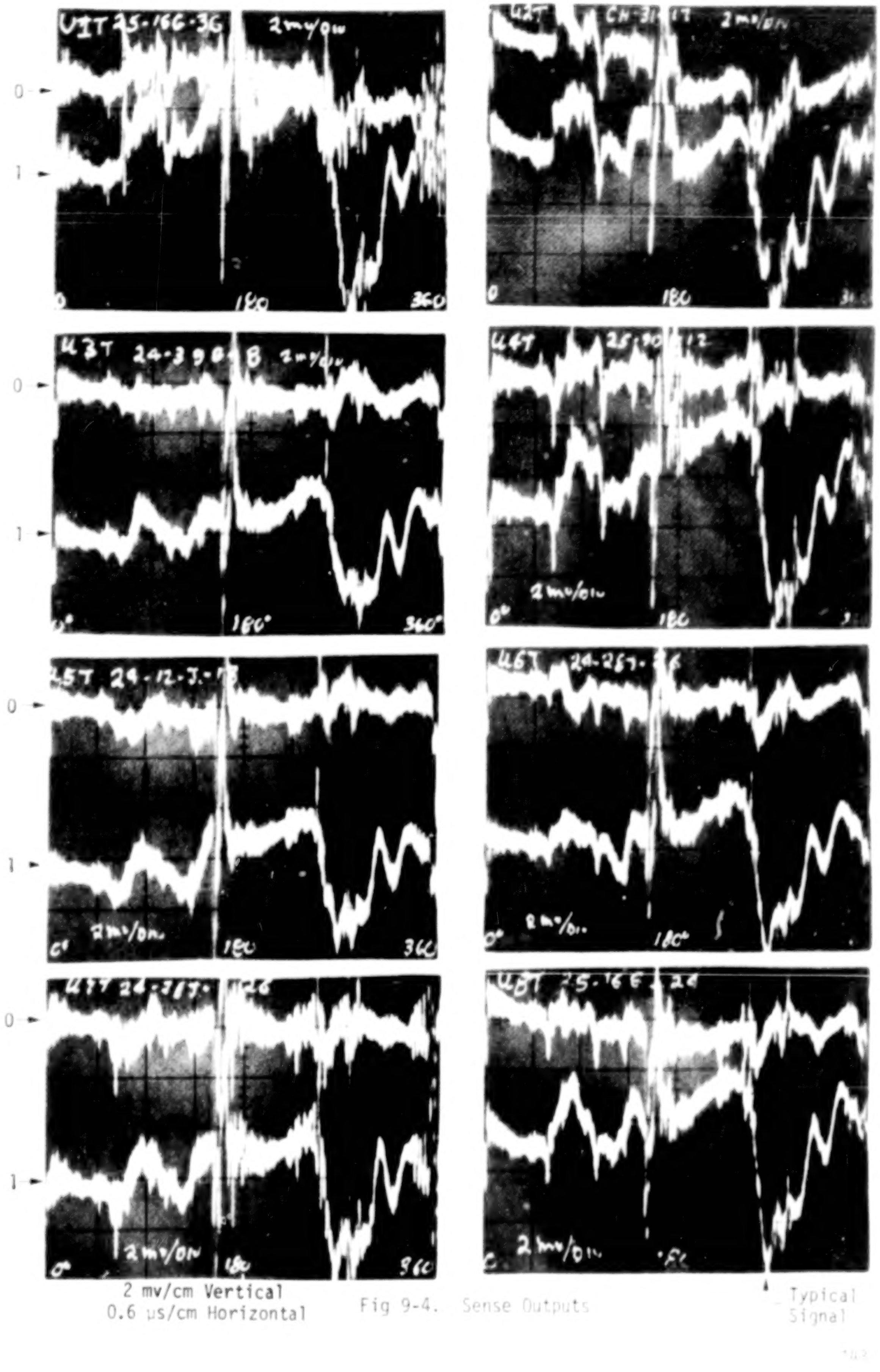
based on a ± standard deviation range of sense parameters. Another contributing factor to sensing problems was a limitation on detector current amplitude. The detector sensitivity of 0.92 mv/ma given in Table 9-1 is measured with a current of 6 ma. As detector current is increased, detector sensitivity remains constant and the output increases until a detector current of about 10 ma is reached. At this point, detector sensitivity starts to decrease with increasing current resulting in an essentially constant output which establishes a maximum available output level. Although the detector signal to noise ratio remains essentially constant as detector current is varied, the net signal to noise improves as detector current and output amplitude increase since cell induced noise amplitude is fixed. Thus a limitation on detector current effectively limits the signal to noise ratio of the cell.

The initial cell design was based on using a detector current of 15 ma which would have resulted in a 50% higher nominal output than that which was achieved. A 15 ma level was selected from preliminary device characterization data reflecting a limitation based on allowable detector power dissipation. The actual detector current limitation encountered during the SSDR program appears to reflect some other phenomena. Investigation of this characteristic has been initiated but the cause of the problem has not yet been identified.

Figure 9-4 is a series of photographs illustrating typical unclamped sense output from all chips on a substrate of a SSDR cell for a "1" and "0" signal.

Because of the various sense problems described in the above paragraphs, it became clear that any attempt to apply test criteria to cell sense signals that would meet the originally established criteria for multiplexed memory element sensing would result in an exceedingly low memory element yield. The cost of attempting to meet such requirements was judged to exceed the value of any information to be gained through such an effort. Initially an undegraded maximum "0" sensitivity of 0.1 mv/ma and a minimum undegraded "1" sensitivity of 1.2 mv/ma was assumed. The data of Table 9-1 indicates actual values obtained were .58 mv/ma for a "1" and 0.14 mv/ma for "0". Based on this data, it was decided to modify the sense channel to accent the type of detector performance indicated in Table 9-1. The modifications made to achieve this are described in Section 10.0.

Another cell parameter of particular interest is the composite bias margin of the memory cells. This relates to how efficiently 16 memory elements may be matched to operate in a common cell. The eight memory cells in the SSDR have a mean available cell bias margin of 6.0 oe with a maximum of 7.7 oe and a minimum of 3.8 oe. The average memory element center bias value is offset from the cell center bias value by 1.05 oe with a standard deviation of 0.775 oe. This implies the average memory element will lose 1 oe from its available bias margin by operating in a cell set or the memory element population mean. The maximum element bias margin reduction based on the applied selection procedure could be practically held to 2.4 oe (2σ). Table 9-2 below summarizes the bias characteristics of the eight cells in the SSDR.



2 mv/cm Vertical
0.6 µs/cm Horizontal

Fig 9-4. Sense Outputs

Typical
Signal

Table 9-2. Cell Bias Characteristics

Cell No.	Bias Level	Bias Margin	Average Element Bias Reduction
1	99.85 oe	6.7 oe	1.05 oe
2	97.25 oe	6.5 oe	1.02 oe
3	91.85 oe	5.9 oe	1.11 oe
4	92.65 oe	7.7 oe	0.41 oe
5	99.66 oe	4.8 oe	1.0 oe
6	96.45 oe	6.1 oe	1.63 oe
7	100.40 oe	3.8 oe	1.26 oe
8	98.75 oe	6.5 oe	0.92 oe

A final area of memory cell test results relates to a series of mechanical environmental tests run on a cell. A tested memory cell was loaded with a known data pattern and subjected to a three axis sine wave vibration test per MIL-STD-810B, Method 514, Part 1, Procedure V, Curve T. After vibration, data was reverified and it was found that one chip was generating errors. This chip was then fully retested and found to have suffered a shift and degradation in operating margin. Cell disassembly and inspection revealed debris on the failed chip surface. After removal of this material, the cell was reassembled and when tested it was found that the margin of the degraded chip had returned to its original level. The cell was then subjected to vibration again and retested with no loss of data or margin degradation.

Based on test data, it was postulated that fine garnet material generated by the laser scribe operation and adhering to the chip edge was loosened during vibration and displaced to the active surface of the chip. If the material contained particles of the magnetic garnet film, the local bias and rotating field could be distorted. This theory was verified by intentionally placing small particles from the edge of a chip on to the active area of a memory element. Tests of the memory elements indicated such contamination did induce failures. To prevent this difficulty, the cell assembly process was modified to include the installation of an 1 mil epoxy preform over the memory element prior to mounting on the substrate. This would provide sufficient separation between any possible magnetic surface contamination and the chip surface to prevent operational degradation.

10.0 MEMORY MODULE TEST RESULTS

10.1 INTRODUCTION

This section summarizes test experience and test results obtained from the two memory modules built for the SSDR. Discussion of this topic will be divided into consideration of operator circuits, sense circuits and coil drive circuits. Each section will consider performance, problems and design modifications made during the checkout process. Also overall memory module performance and test results are discussed and summarized.

10.2 OPERATOR CIRCUITS

As discussed in Section 5.0, the operator circuits consist of drivers and matrix selection switches required to provide annihilator and generator currents to the memory elements of the addressed cell. In general, the approach and circuit designs used to generate these functions are straightforward and only one significant problem was encountered. This was related to overshoot of the annihilator current waveform which under certain conditions would result in nucleation of a bubble in the area outside of the annihilator current loop where the annihilate field subtracts from the bias field. Cause of this difficulty was the very fast rise time of the voltage on the base of the current source output transistor. The impedance in the voltage clamp line allowed the base voltage to overshoot resulting in an annihilator current overshoot. A 100 pf capacitor was connected between the base and -5 volts to increase the rise time sufficiently to allow effective clamping of this point.

10.3 SENSE CIRCUITS

In checkout of the SSDR, sensing was clearly the major problem area encountered. These sense problems arose from two primary sources; basic problems associated with the sense channel design and detector characteristics which failed to meet parameters that were assumed for purposes of sense channel design.

Fundamental design problems encountered in checkout of the sense channel included oscillation associated with the detector current source drivers, noise coupled into the sense channel and a common to difference mode conversion within the sense channel.

As described in Section 5.0, current sources are used to provide current to the active and dummy detector of the memory elements in the addressed cell as established by the sense select switch. These current sources are then required to drive the sense bus which connects the thirty-two cells on the module. Associated with this bus is a capacitance to ground of 390 pF. This capacitance, which was greater than estimated for initial design purposes, was sufficient to cause the current sources to oscillate at a frequency on the order of 100 MHz. A solution to this problem involved adding a 47 pF capacitor from collector to base of each current source. This capacitance provides sufficient degeneration to inhibit oscillation. Figure 10-1 illustrates this modification.

The high sense bus capacitance resulted in another problem beyond current source oscillation. When the current sources are turned on, the sense bus will charge toward its steady state value with a time constant determined by the bus capacitance and detector resistance. Based on measured parameters, the sense bus charges toward about 6 volts with a 200 μs time constant. System timing allows 1.25 μs for the sense bus to settle before the clamp in the A.C. coupled sense amp is released. Although this time corresponds to about six time constants, the bus charging voltage is 6 volts compared to the sense signal level which is on the order of 5 millivolts. Because of this, the sense bus is still moving an appreciable amount compared to the sense signal at clamp release time. As long as this motion is common mode, as would be the case if sense and dummy bus capacitance, resistance and current are identical, no problem results. However any unbalance in these three parameters results in a common to difference mode conversion which is seen by the sense amplifier. Figure 10-2 illustrates the common mode voltage seen by the sense amplifier during sense time.

Of the three variables effecting a conversion of this common mode voltage, two may be controlled. Both current unbalance and bus capacitance unbalance are constant for all cells in the module and may be either adjusted to be balanced or compensated for by the sense amp threshold voltage setting. However detector/dummy resistive balance is variable from cell to cell and cannot be easily compensated. Data from the memory elements in the SSDR indicate a mean unbalance of 2.2Ω with a standard deviation of 8.7Ω. This unbalance is capable of generating difference mode error signals at the sense amplifier on the millivolt level which may be either positive or negative and effectively prevent a common sense threshold setting for all chips. Additionally, the detector impedance and sense bus capacitance establish the effective bandwidth of the sense channel. The sense bus had a 700 KHz bandwidth which resulted in applicable signal attenuation. To minimize these present problems during completion of testing of the SSDR, it was decided to physically cut the sense bus on the sense/operator MLB such that the bus would only be connected to 16 cells rather than 32. Since the memory module was only partially populated, this modification did not affect capability but did serve to cut sense bus capacitance to about 180 pF and minimize sense offsets from this source.

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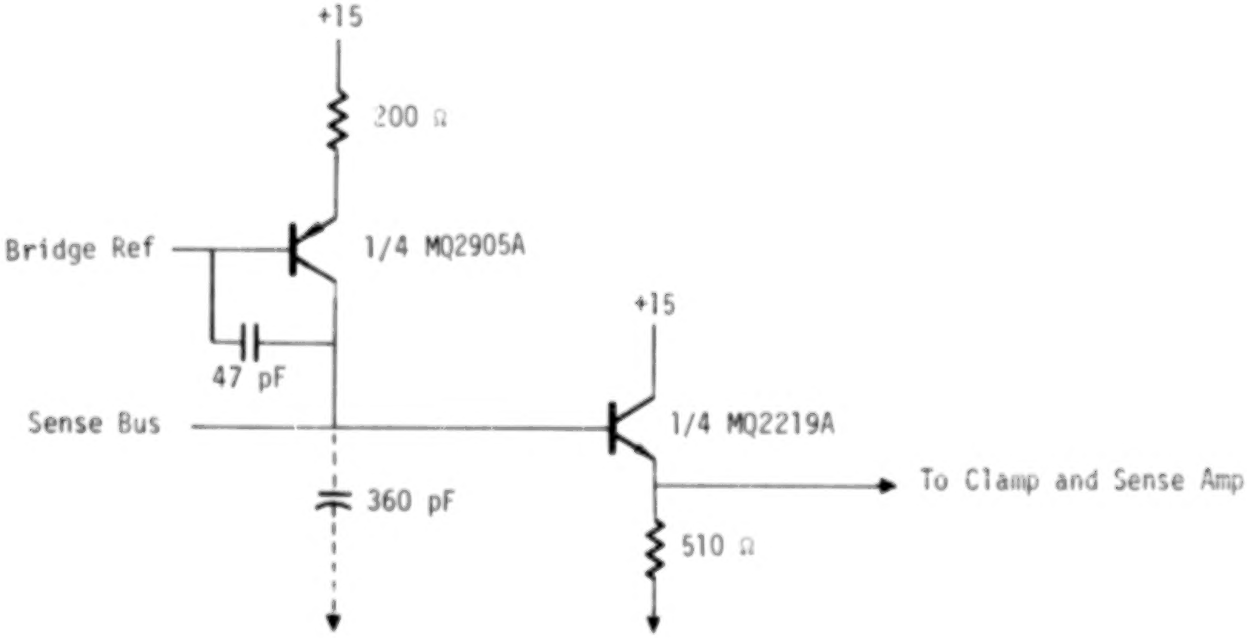

+15
200 Ω
Bridge Ref
1/4 MQ2905A
+15
47 pF
Sense Bus
1/4 MQ2219A
To Clamp and Sense Amp
360 pF
510 Ω

Figure 10-1. Current Source Modification

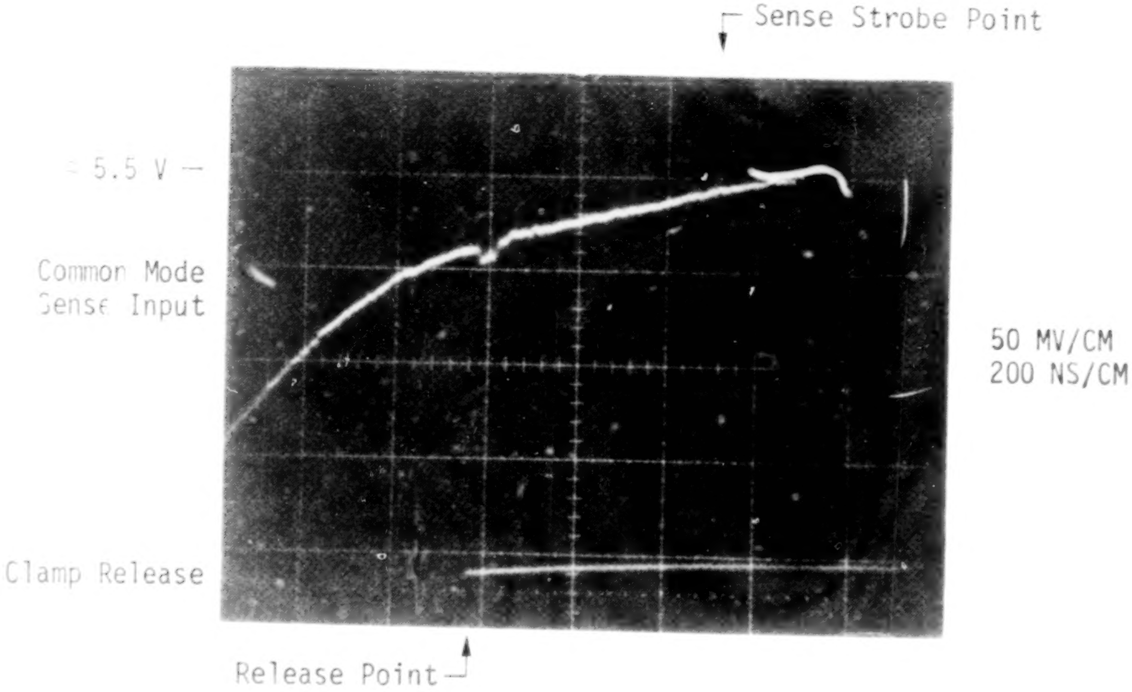


Fig 10-2. Sense Amp Common Mode Voltage at Sense Time

A final sense channel design problem encountered during checkout was associated with noise coupled into the sense channel. The source of this noise was logic signal transitions which took place during the clamp release sense time and were capacitively coupled into the sense bus. Although during layout of the 10 layer sense/operator MLB, care was taken to isolate the sense bus as much as possible, the exceedingly high interconnect density (on the order of 7,000 interconnects) forced compromise in some areas that resulted in subsequent noise problems. The alternatives were to increase the number of board layers or significantly increase board size with both being considered undesireable. During checkout, noise problems from this source were eliminated by identifying, cutting and hardwiring the noise inducing signals onto the MLB surface.

In addition to the design problems discussed above, a fundamental problem was encountered in terms of the ability of the memory element detector to operate in a matrixed sense configuration. As additional cells were added to the memory module, it became clear (as was also indicated in cell test) that there did not exist a single sense threshold setting that would result in proper operation for any appreciable number of cells. This problem results from a combination of factors associated with the detector output amplitude for a bubble, no bubble and adjacent bubble. The signal amplitude generated by the detector when a bubble is present is a fundamental property of the detector and is generally expressed in terms of millivolts/milliamp of detector current. Based on preliminary chip characterization data, sense channel design assumed a 15 ma detector current could be used with further increases in detector drive limited by dissipation in the detector. However as memory elements were fabricated for the SSDR, test results indicated that no increase in output amplitude was achieved for currents about 10 ma with the limitation apparently due to some mechanism other than heat due to power dissipation. This then resulted in a 33% reduction of the assumed available output. In addition, as indicated in Section 9.0, a considerable chip to chip variation in sensitivity in the linear region below 10 ma was encountered resulting in a further decrease in available signal.

The low available signal resulted in two problems. First and most obvious was the degradation of signal to noise ratio for the sense channel. A second problem was associated with sense amplifier characteristics. The SN55236 sense amp was selected because of its good sensitivity at low signal levels (specified to 5 mv) and adjustable threshold with both of these characteristics being required for the low level unipolar signal generated by the bubble chip. However, due to the sense signal amplitude available it was found threshold settings at or below the specified 5 mv level were required. As illustrated by the data on sixteen sense amps presented in Figure 10-3, attempting to operate the amplifier in this range (dotted line) resulted in erratic performance.

In addition to the problems with signal amplitude described above, the no bubble signal amplitude variation also presented additional sense margin problems. Nonzero no bubble signals arise from two sources, dynamic mismatch between dummy and active detectors and signals generated by bubbles adjacent to the detector (prior to or after the detector). The type of variation experienced due to adjacent bit detection is illustrated in Figure 10-4.

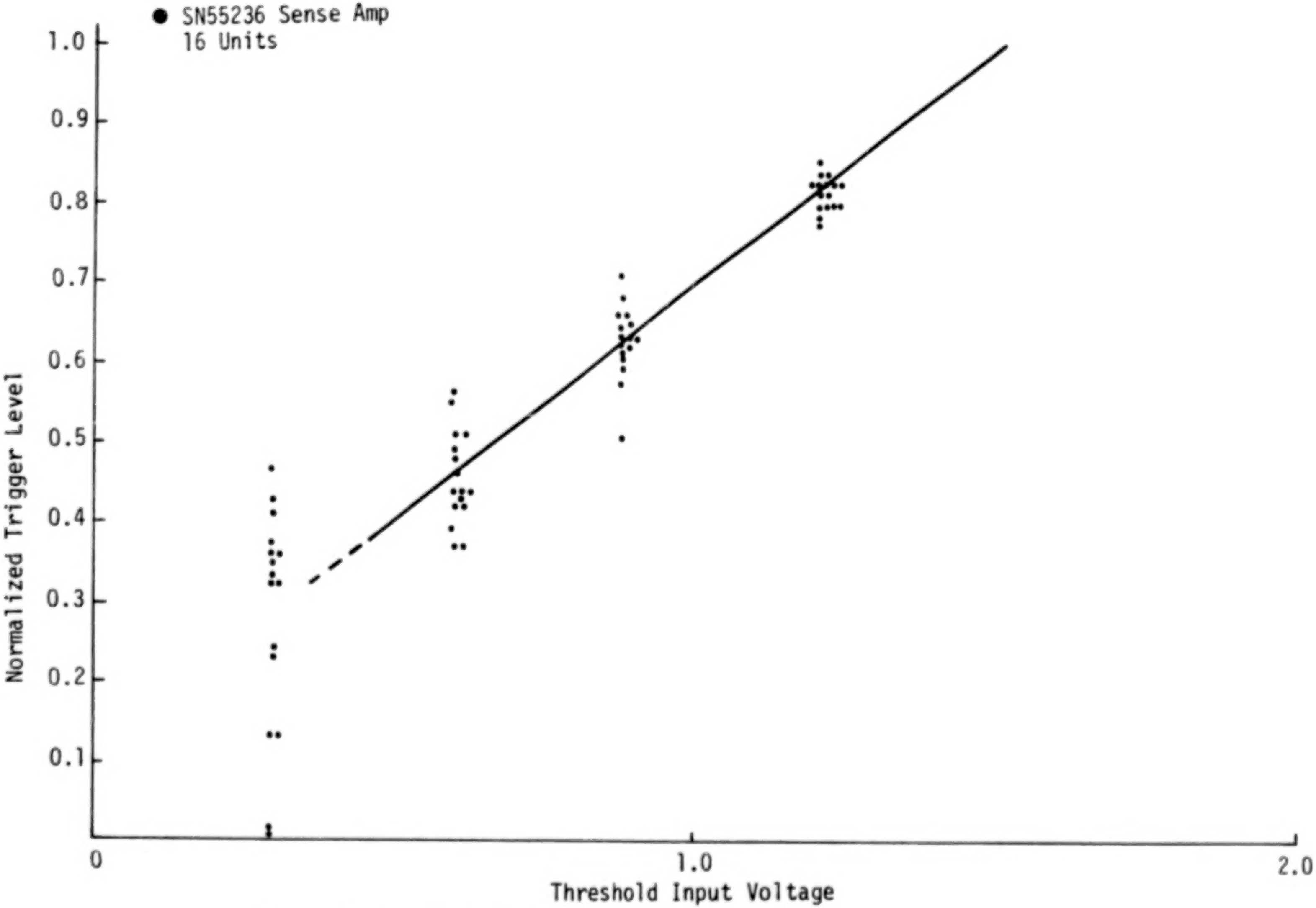
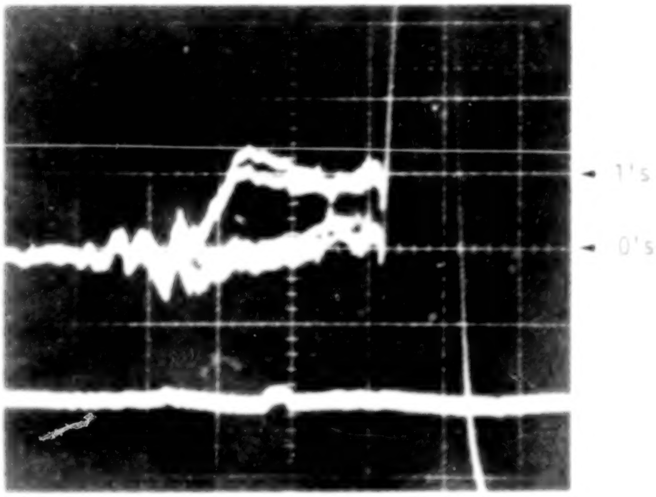
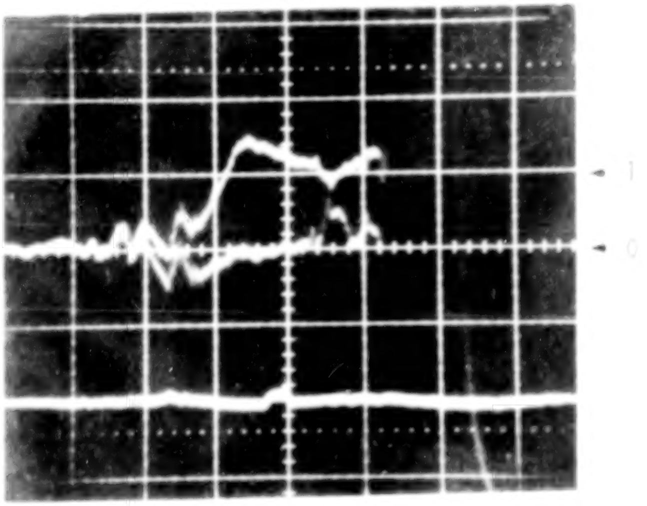


Figure 10-3. Sense Amp - Threshold Characteristics

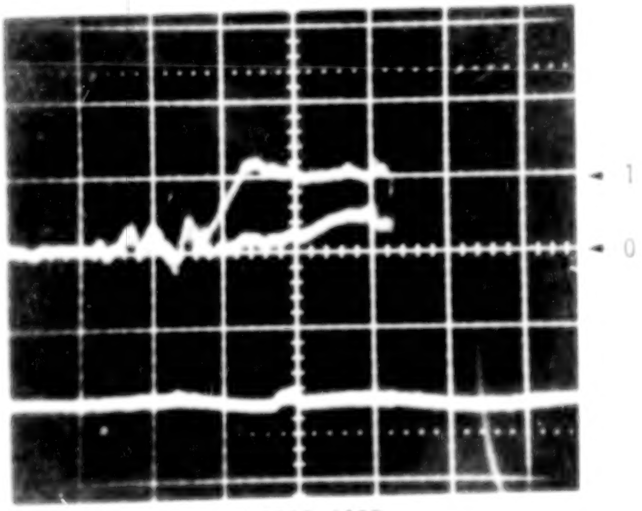


CELL 12
BIT 4
5 MV/DIV VERTICAL
200 NS/DIV HORIZONTAL
0001111100110010

ALL BITS



BEST CASE



WORST CASE

Fig 10-4. Adjacent Bit Effects

When all of the factors described above are considered in terms of a sense analysis, the result is that the combination of low output and high and variable no-bubble signal made multiplexing a single fixed threshold sense amplifier over many memory elements impractical. Plans for testing the SSDR called for populating one memory module with two cells and the second memory module with six cells. It was possible to establish a threshold allowing sense amps multiplexing for the two cell module but a common setting for the six cell module was not feasible. In order to allow SSDR evaluation to be completed using all cells, it was decided to add a modification to the six cell memory module which would program the sense amp threshold based on the cell addressed. This allowed a sense threshold setting which was optimum for each memory element. The circuit used to implement this approach is illustrated in the schematic of Figure 10-5. The threshold for a particular sense amp is established by one of six selected resistors with each resistor corresponding to one of the six cells. The resistor to be used is established by a cell address term which applies a reference voltage to the resistors associated with that cell for all bits. This circuit was physically implemented using a circuit board which was mounted in the unused cell mounting area of the memory module. This circuit functioned as intended and allowed use of all six cells on the memory module.

10.4 COIL DRIVE CIRCUITS

The matrixed coil drive system operated in a fundamentally satisfactory manner. Only one significant problem arose with this circuit during memory module checkout. The first problem related to sense strobe timing. It was found that differences in turn off storage time between the voltage switches in the coil drive matrix resulted in a relative timing shift in the drive current wave form depending on the particular switches used. This problem is illustrated by the waveforms of Figure 10-6 which illustrate the shift in sense signal and drive current timing between two cells. Because of the position in the cycle of the sense signal, X current timing changes are reflected almost one to one in a shift in sense signal timing (as illustrated in Figure 10-6). To eliminate this problem, the sense strobe was generated internal to the memory module from the coil drive voltage transition associated with the positive going X current inflection shown in Figure 10-6. A circuit to generate this function was included in the initial coil drive design but fixed strobe timing was used until the extent of the problem became clear. Figure 10-7 illustrates how this technique keeps the sense strobe centered on the sense signal with timing shifts in drive current.

10.5 MEMORY MODULE TEST RESULTS

After checkout and modification of the memory module as described above, a series of tests were run to characterize memory module operation. Power consumption of the memory module as a function of data rate is given for a write operation in Figure 10-8 and for a read operation in Figure 10-9. The significant difference between 2 cycle burst read and 16 cycle burst read power is due the one cycle precharge required for first bit detection. In one case this precharge power is averaged over two cycles as compared with sixteen cycles for the longer burst.

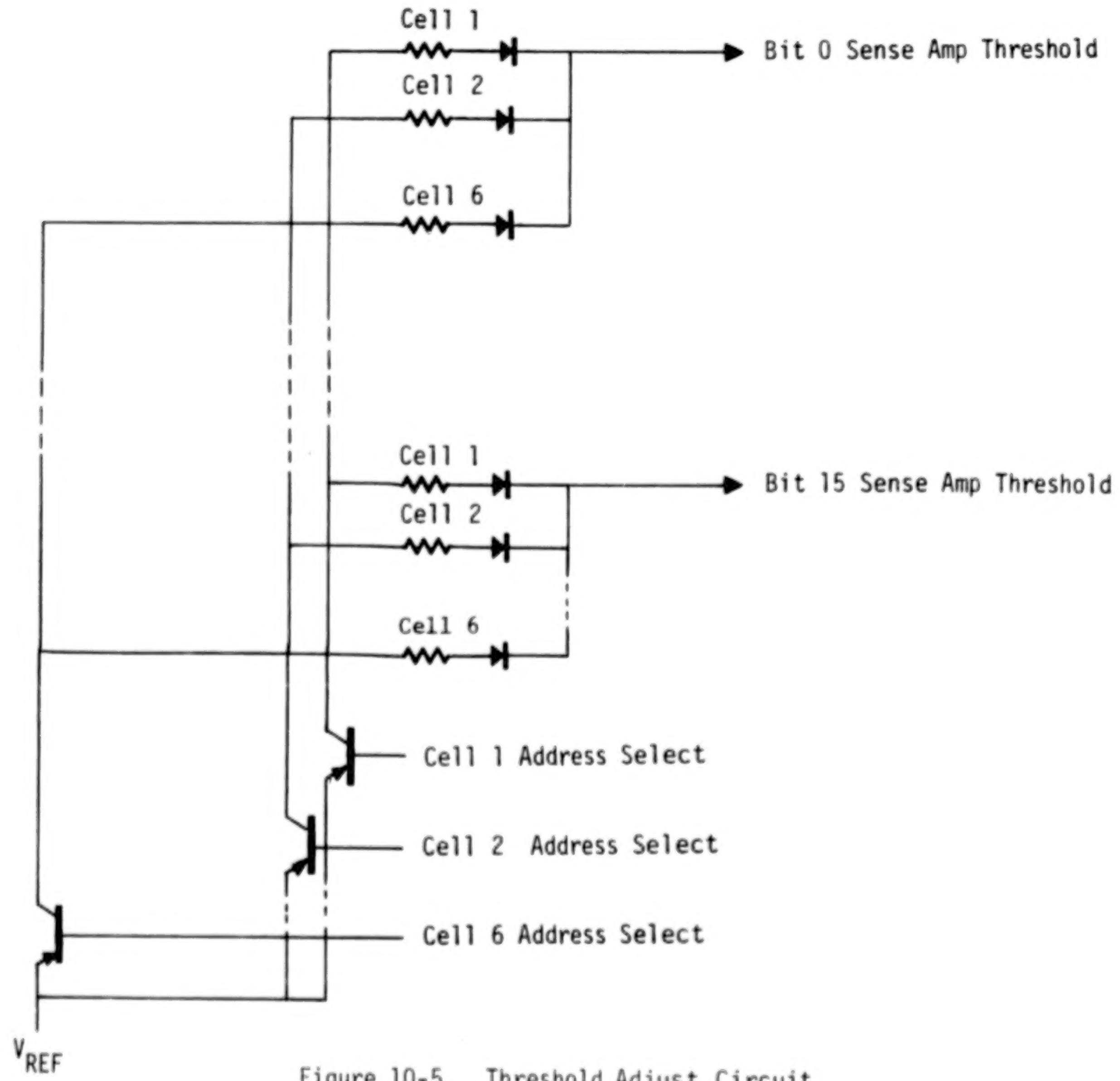

Cell 1
Bit 0 Sense Amp Threshold
Cell 2
Cell 6
Cell 1
Bit 15 Sense Amp Threshold
Cell 2
Cell 6
Cell 1 Address Select
Cell 2 Address Select
Cell 6 Address Select
V_{REF}

Figure 10-5. Threshold Adjust Circuit

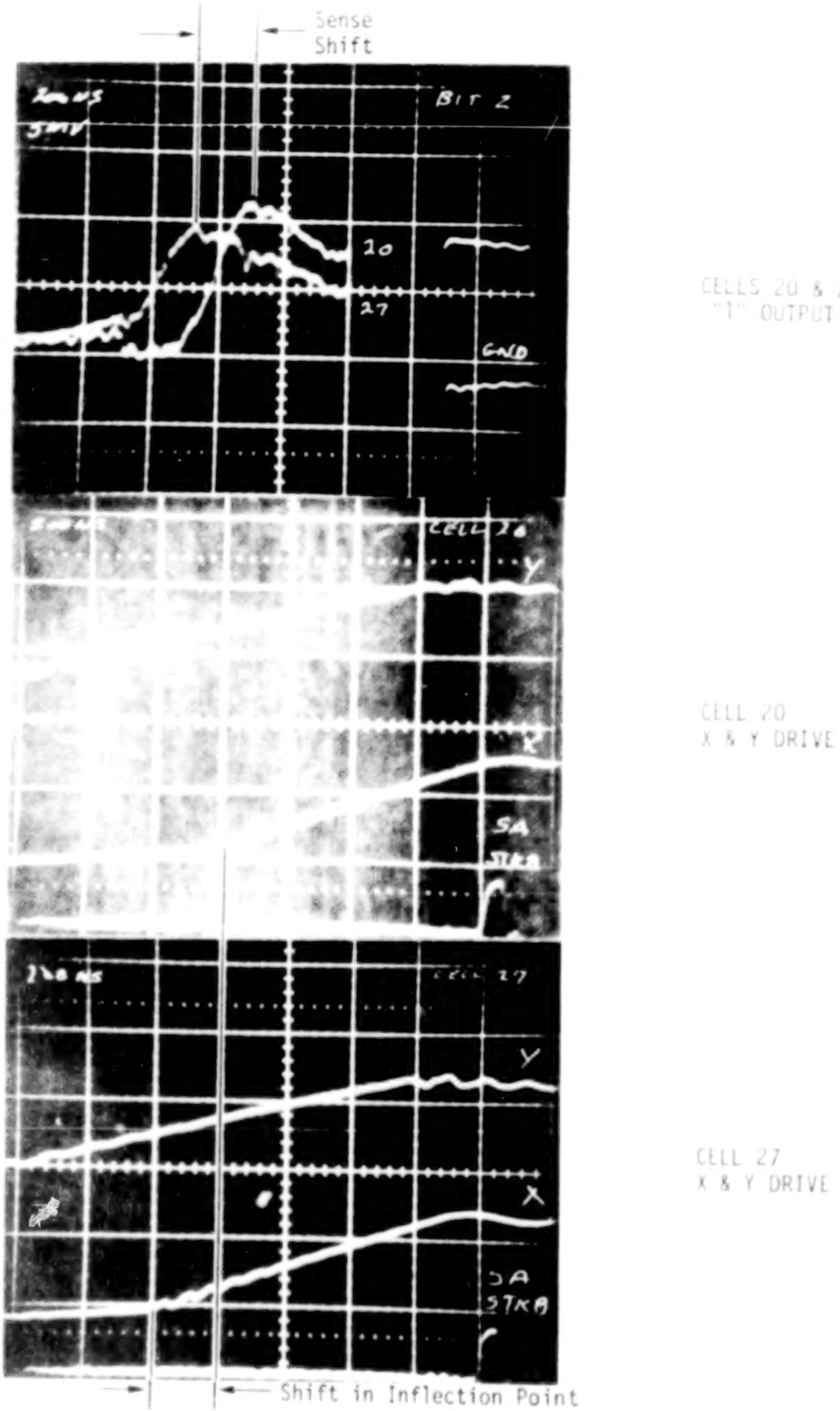


Fig 10-6. Sense Signal Timing Variation

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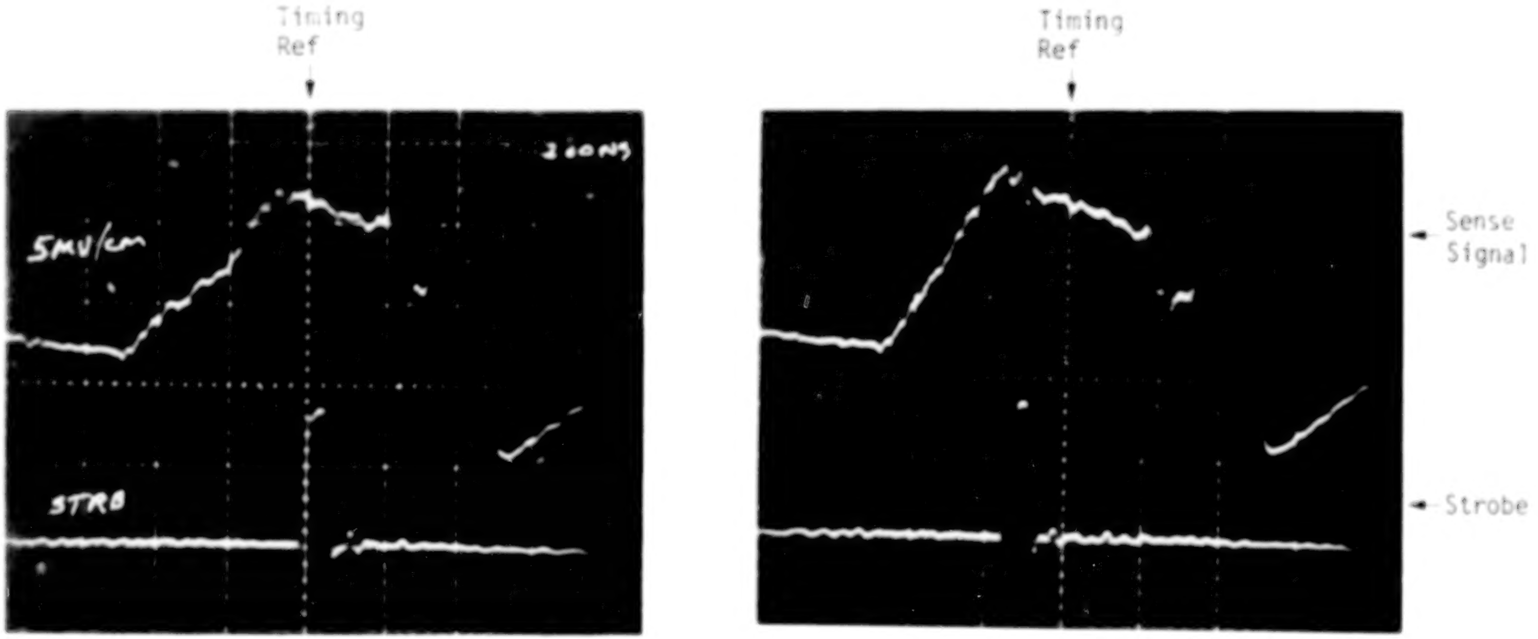

CELL 20

CELL 27

Fig 10-7. Drive Generated Strobe Timing

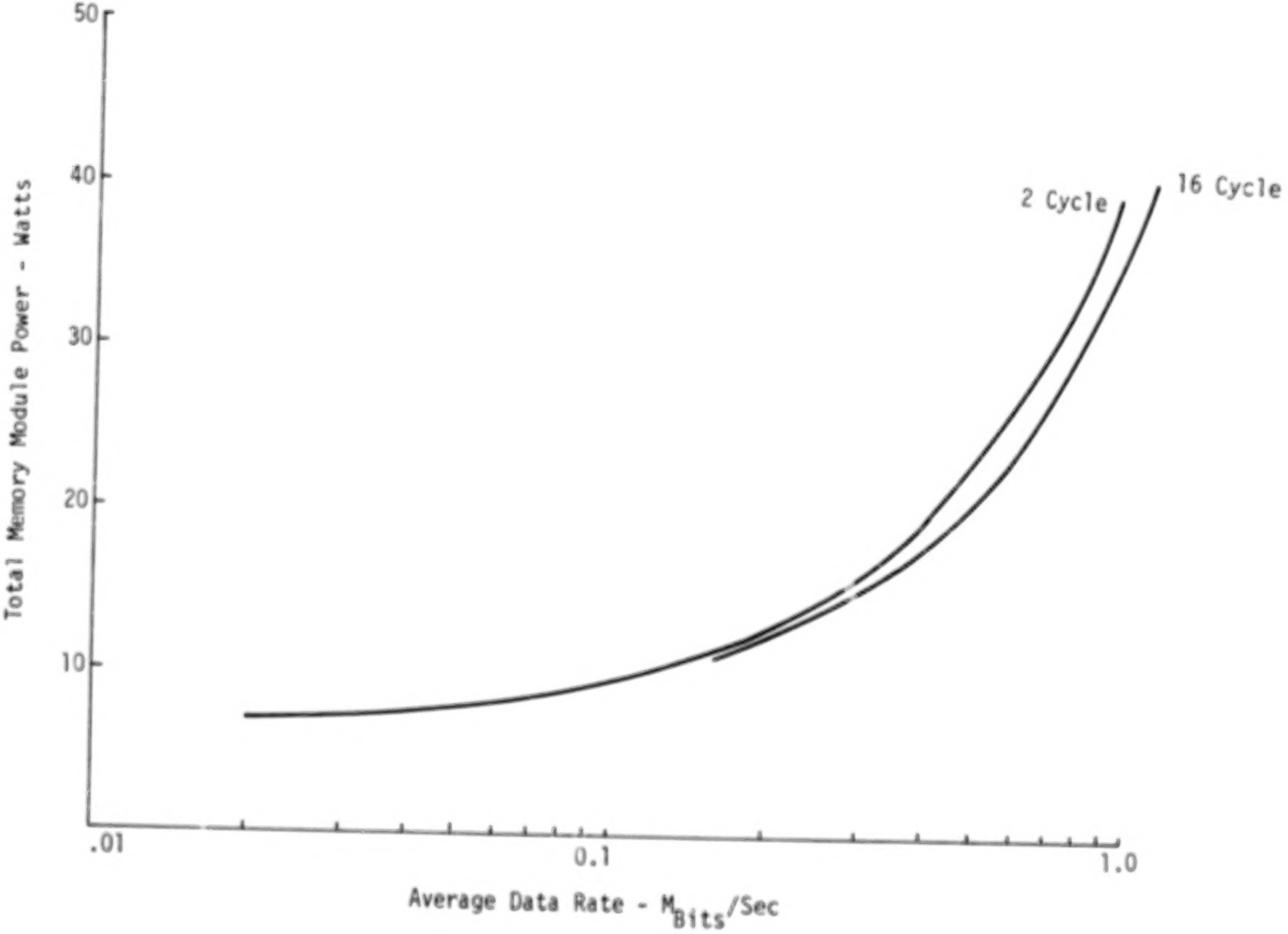

Figure 10-8. Write Power

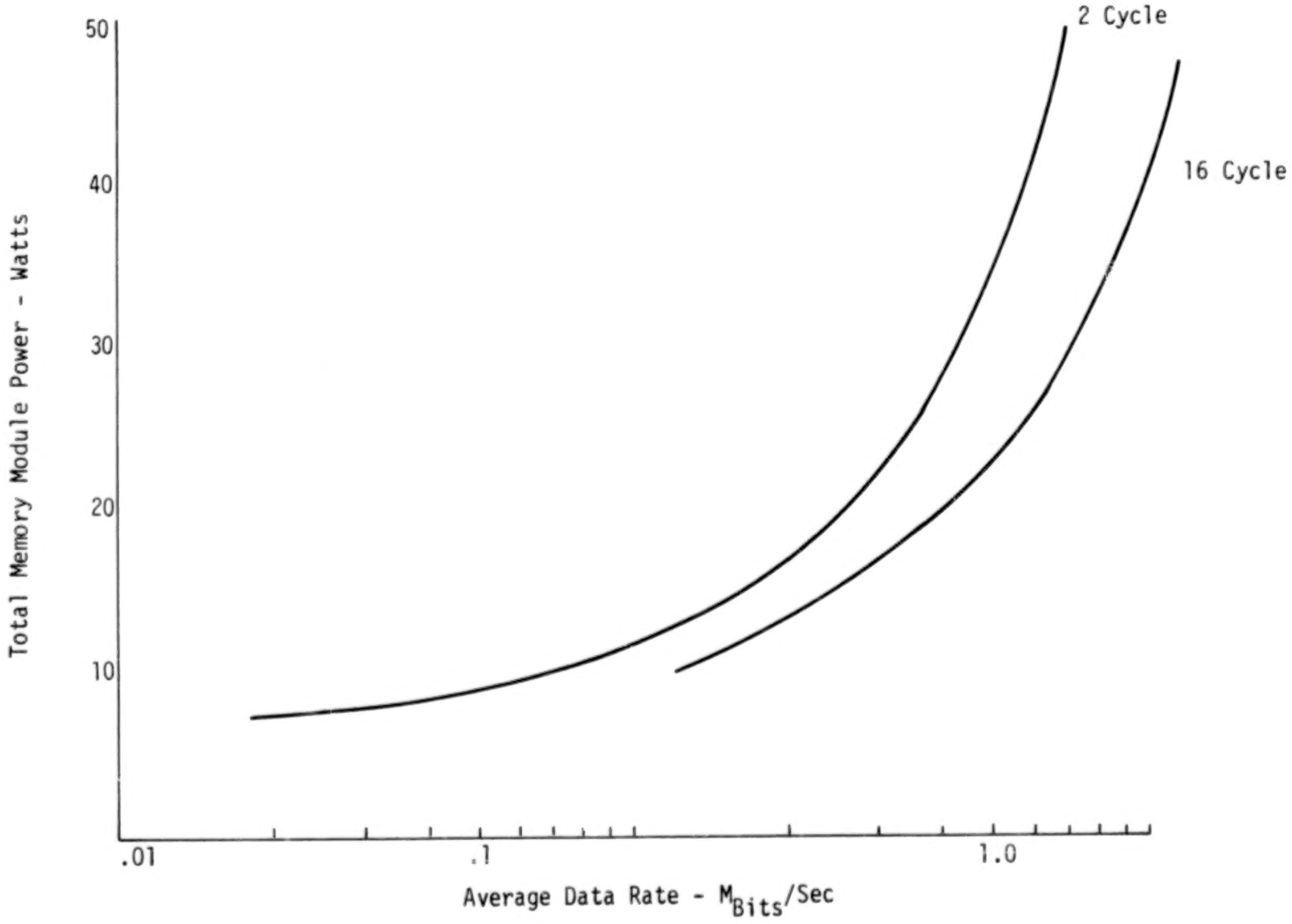

Figure 10-9. Read Power

The memory module was operationally tested in terms of both a magnetic and temperature environment. Read and write operations were performed in ambient D.C. magnetic fields of 30 oe on all memory module axes without measureable effect on memory module operation. Temperature tests were run to determine both operating and nonvolatile storage temperature range. As discussed in the cell test results of Section 9.0, it was necessary to limit the cell operating temperature to 0°C to 50°C for purposes of cell acceptance testing. Memory module performance would be expected to reflect this range less any degradation introduced by the memory module environment. Operating temperature tests indicated a module operating temperature range of about 0°C to 45°C. Temperatures significantly above this point resulted in a significant increase in error rate. These errors primarily resulted from a reduction in available sense margin due to lower detector sensitivity at high temperatures.

Performance of the memory module was also evaluated as a function of coil drive voltage to establish available drive field margin at the memory module level. With a nominal setting of 60 volts, a minimum operating voltage of 54 volts and a maximum operating voltage of 70.5 volts was measured. This corresponds to a +16.77, -10% operating margin for coil drive voltage which agrees with expected performance. The offset voltage tolerance results from selecting a nominal operating voltage as slow as possible to minimize coil drive power.

11.0 DCU TEST RESULTS

11.1 INTRODUCTION

This section summarizes checkout and test of the DCU hardware and software prior to final SSDR system integration. The initial test configuration used for the DCU is illustrated in Figure 11-1. Testing was done using a PDP-11 based computer controlled tester. Lab power supplies, which allowed voltage margin testing, were connected to the DCU via a power supply junction box (J-Box) which provided DCU initialization, power on-off control and voltage/current monitoring. The J-Box between tester and DCU allowed electrical access to all interface lines and provided configuration control for the DCU. Initial checkout was done using two PPS microprocessor development systems (assemulators) in place of the channel controller microcomputers. This approach provided a maximum amount of test experience prior to committing to the fabrication of software ROM's for the channel controller.

11.2 DCU CHECKOUT

Initial checkout of the DCU involved driving the various DCU subsections with the SSDR software to perform the command control and data manipulation necessary to achieve SSDR channel operation. Basic communication between the DCU and the computerized test equipment was established. The DCU and test equipment were operated in a "wraparound" mode as illustrated in Figure 11-2 to verify and test data transfer between user and DCU with the test equipment simulating the Memory Module.

After initial basic functional checkout of the DCU, compatibility between DCU and the Memory Module was established by integrating a memory module containing one cell with DCU. This allowed verification and finalization of the timing control PROM in the DCU memory module controller. Signal level, polarity and timing were verified for operation selection, cell selection, coil drive and data interface. The memory element address hardware/software module was verified by partially writing the cell and issuing a STOP command prior to the EOC. The READ command then aligned the cell to BOC and read the cell up to the write pointer at which point the operation would automatically stop. Comparison of the data pattern read with that stored verified proper memory element address control.

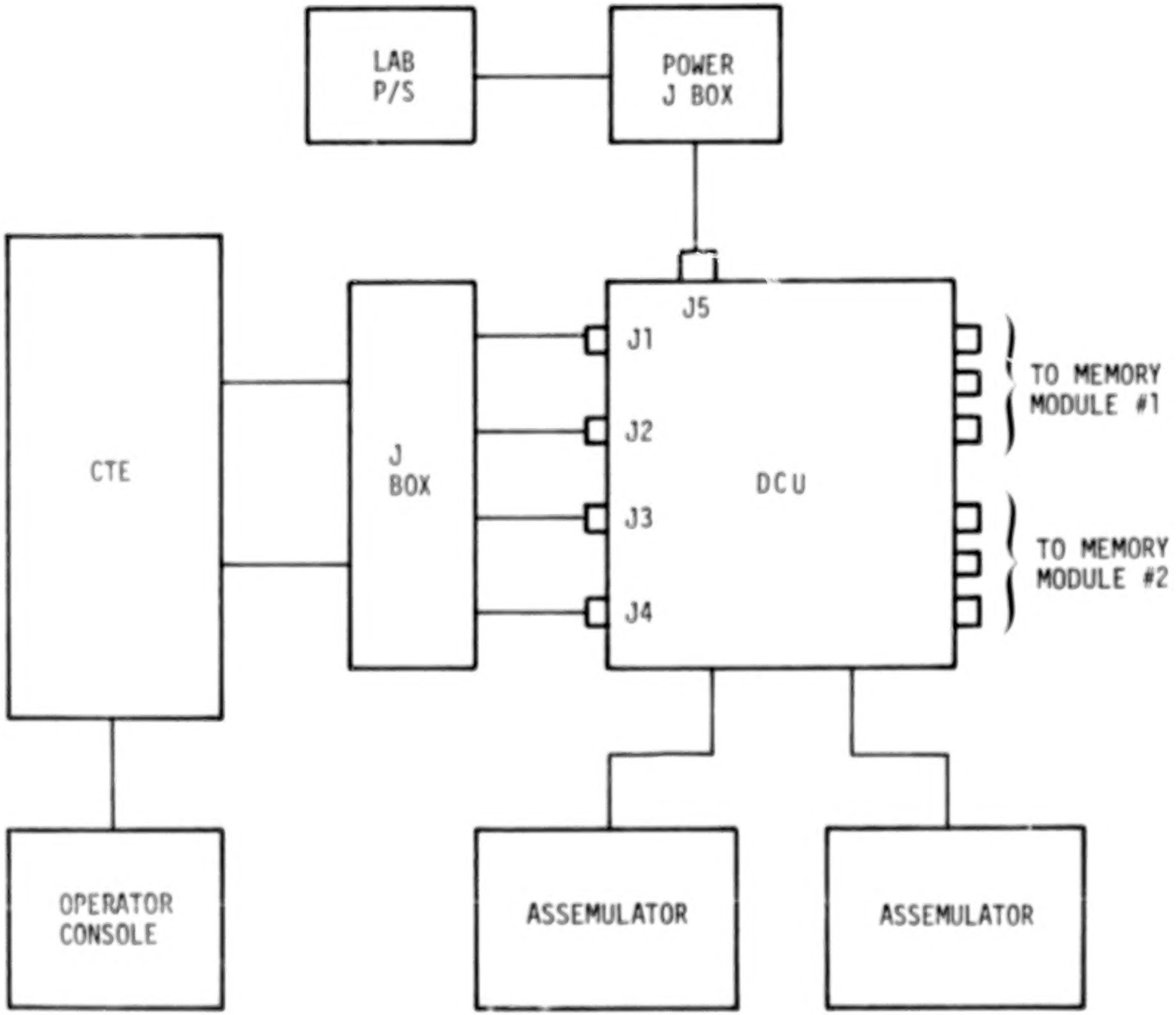
LAB
P/S
POWER
J BOX
CTE
J
BOX
J5
J1
J2
J3
J4
DCU
TO MEMORY
MODULE #1
TO MEMORY
MODULE #2
OPERATOR
CONSOLE
ASSEMULATOR
ASSEMULATOR

Figure 11-1. DCU Test Configuration

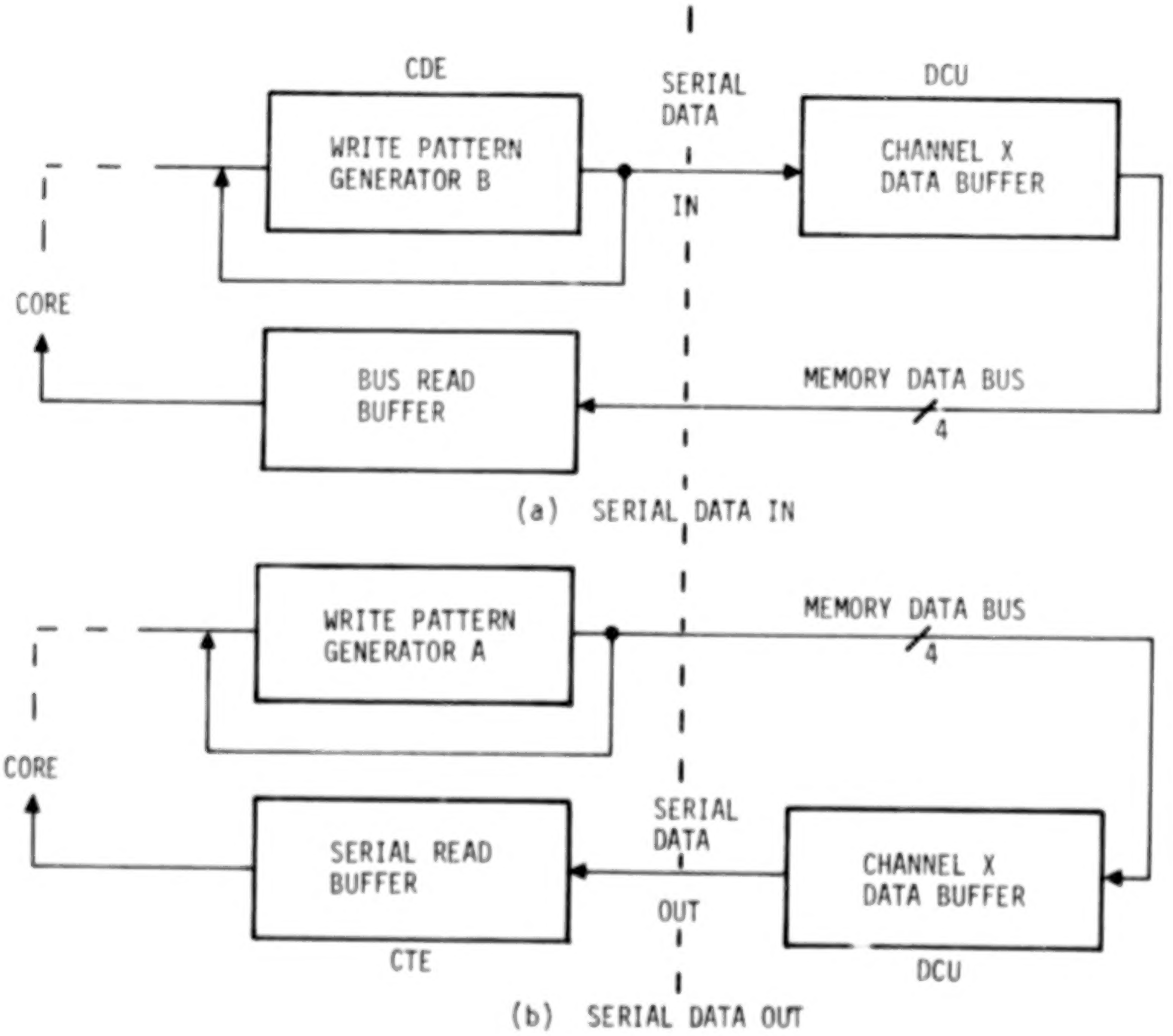
CDE
SERIAL DATA
DCU
WRITE PATTERN GENERATOR B
CHANNEL X DATA BUFFER
IN
CORE
BUS READ BUFFER
MEMORY DATA BUS
4
(a) SERIAL DATA IN
WRITE PATTERN GENERATOR A
MEMORY DATA BUS
4
CORE
SERIAL DATA
SERIAL READ BUFFER
CHANNEL X DATA BUFFER
OUT
CTE
DCU
(b) SERIAL DATA OUT

Figure 11-2. Data Buffer Test Configurations

The major problem that existed with the software at this juncture was unreliable DCU to memory module data transfers at high system data rates. The problem was addressed by performing an analysis of various software sequence operating times to determine if operating speed was software limited. In addition, a detailed functional analysis of the DCU software operation using a logic analyzer was undertaken.

During the software testing process, two channel controllers, two channel data buffers and both memory module controllers were fully exercised with a memory module attached. Problems with multiple and simultaneous hardware interrupts were found and rectified. The major obstacle to overcome during finalization of the DCU software was continuous operation (Read or Write) over multiple cells at high data rates. In an effort to speed up the software, the automatic updating of telemetry status during Read or Write operations was eliminated. In the final analysis, it was determined that for the present DCU software/hardware design, continuous operation over multiple memory cells at data rates greater than 1.0 Mbps single channel or 2.0 Mbs composite is unreliable. During Read and Write operations, two program interrupts are active. The first is the Data Buffer Service interrupt which occurs whenever the FIFO channel data buffer requires service, i.e., filled from the memory module during a Read operation or emptied to a memory module during a Write operation. The second is the Cycle Counter Overflow interrupt which occurs whenever the 8 bit memory module cycle counter overflows. The first interrupt causes the DCU channel controller to initiate the servicing of the data buffer. The second interrupt causes the channel controller to update the memory element address and control the transition from cell to cell in multiple cell operations. During the transition between cells, the cycle counter overflow interrupt program execution is especially long causing the data buffer to overflow, losing data at cell boundries for data transfer rates greater than 1 MHz. This maximum limit, which applies only to multiple cell operations, can be increased by increasing the size of the FIFO data buffer or by initiating data buffer service entirely by hardware, eliminating the first interrupt.

12.0 SYSTEM TEST RESULTS

12.1 INTRODUCTION

This section discusses results of the final SSDR system integration and test. System test was limited to basically a verification of system function in the various operating modes and evaluation of the operating parameters of power consumption and error rate. A decision was made to eliminate planned system environmental tests from the program. This was based on the fact that the limited temperature range and marginal sense performance of the Memory Module would certainly be the limiting factors in system performance. Under these circumstances, it did not seem useful to spend additional time and money to determine performance limits which had been effectively established previously at the Memory Module level. The following sections summarize the SSDR integration experience and present nominal performance data obtained in checkout and evaluation.

12.2 SYSTEM INTEGRATION

Final system integration of the component parts of the SSDR system was accomplished with minimal difficulty. DCU-Memory Module compatibility tests run prior to integration resolved most problems. The only basic problem uncovered during integration and test was a data pattern sensitivity in the Memory Module which had not been observed previously. The data pattern sensitivity observed at system integration was both lost "1"'s and "0"'s in approximately equal numbers using the same test pattern used at the Memory Module test except the data pattern was shifted one bit for each chip. It was further observed that the errors were caused by certain chips in a given cell. These chips correlated very well to chips causing low sense margins at Memory Module test. And the failures occurred at points where maximum zero noise or minimum one signal normally occurred. The maximum zero noise always occurred in any data pattern where two or more zeros preceded or followed two or more ones with the zero adjacent to a one having the largest noise. And the minimum one occurred where it was the last "one" in a string of two or more "1"'s.

Investigation indicated the pattern sensitivity was due to noise coupling from sense amp to sense amp through the power bus on the sense MLB. The low available sense margin combined with the marginal capability of the sense amp to operate at the required threshold settings (See Section 5.0) caused the sense amps to be very sensitive to power supply noise. This sensitivity was further aggravated by the power switching used on the sense amps to minimize power consumption. Because of turn-on surge current through the switches, the amount of local decoupling capacitance that could be used was limited. In order to improve sense performance, power switching was removed from the sense amps allowing additional power supply decoupling to be added to the sense amplifiers. Although some cell byte pattern sensitivity was still discernible in error rate measurement, the effect was significantly reduced by this modification.

12.3 SYSTEM TEST

In addition to basic function, the primary evaluation criteria for the SSDR system was error rate. A series of tests were run utilizing worst case data patterns to establish system error rates at room temperature. Based on the eight cells contained in the SSDR system, an average system error rate of 9.6×10^{-5} errors/bit was obtained. Error rates on a cell basis are summarized in Table 12-1 below.

Table 12-1. Error Rates on a Cell Basis

Cell	Error Rate
1	4.8×10^{-5} errors/bit
2	1.6×10^{-5} errors/bit
3	0.12×10^{-5} errors/bit
4	1.0×10^{-5} errors/bit
5	0.23×10^{-5} errors/bit
6	2.8×10^{-5} errors/bit
7	61.5×10^{-5} errors/bit
8	0.03×10^{-5} errors/bit

Analysis of these tests results indicated that the errors measured were essentially soft or sensing errors as opposed to hard or data storage errors. The error rate also tends to be pattern sensitivity reflecting the sense amp to sense amp noise coupling discussed previously in this section and the adjacent bit detector noise discussed in Section 9.0. Basically this soft error rate reflects the marginal nature of the total sense channel configuration including both sense circuit design and detector characteristics.

Data was also taken on system power as a function of various operating conditions. Figure 12-1 illustrates how primary power varies as a function of total composite system data rate for a read and write operation. A more detailed breakdown of power consumption is given by the curves of Figure 12-2 for data rates up to 1 M bits/s. This data clearly indicates that the relatively high power at low data rates is primarily due to power supply loss. Switching regulations of the type used in the SSDR power supply have a fixed power consumption overhead which is a function of the peak power required and relatively independent of secondary power. As discussed in Section 7.0, cost considerations led to use of a relatively inefficient power supply design. A customer power supply operating at 80% efficiency could reduce the low data rate primary power requirements by about 1 amp.

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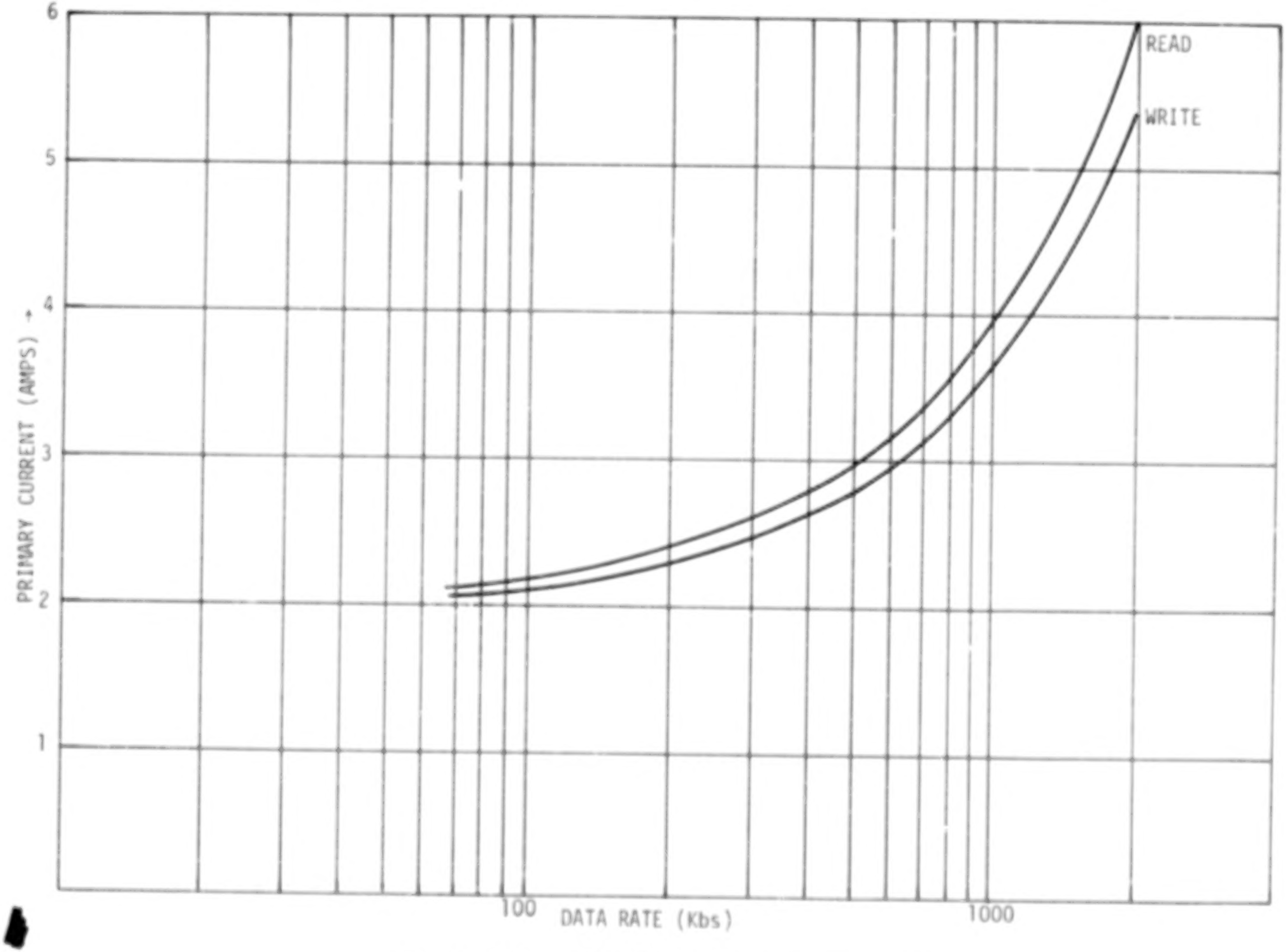

Figure 12-1. SSDR Primary Power Requirements

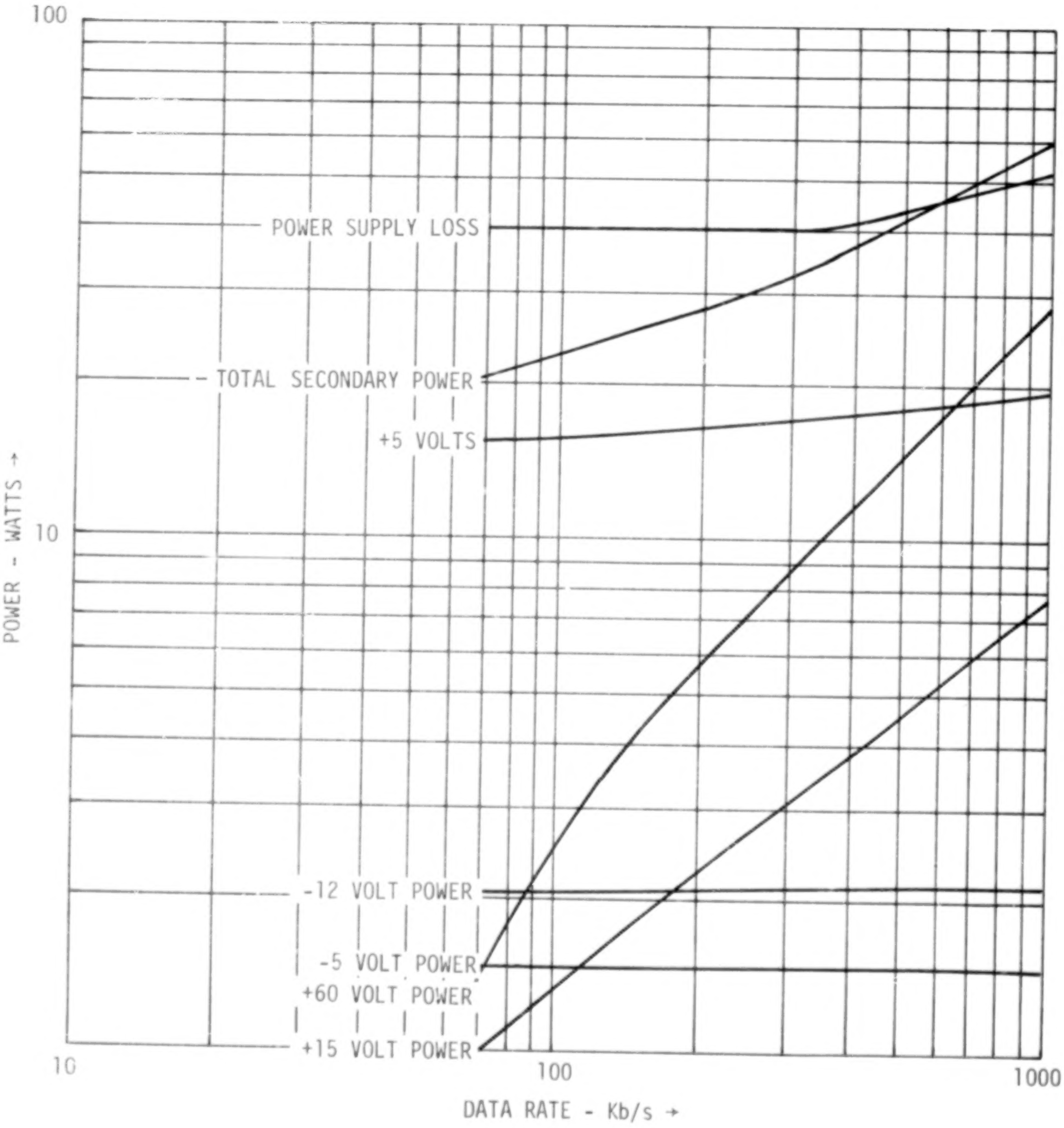

Figure 12-2. System Power Breakdown

13.0 SUMMARY AND RECOMMENDATIONS

13.1 INTRODUCTION

The experience gained in the design, fabrication and test of the SSDR System has significantly contributed to the body of knowledge available which is relevant to the application of bubble memory technology to spacecraft use. Although a number of problems were encountered, these problems are understood and solutions available. In total, the SSDR has served to substantially develop and demonstrate the techniques and feasibility of bubble domain memory technology for spacecraft applications. Based on data and knowledge gained from this program along with parallel improvements in memory element technology that have occurred, it is now possible to undertake the design and fabrication of bubble memory flight hardware for space applications. The remainder of this section discusses accomplishments, problems and recommendations for design modifications for future systems.

13.2 PROGRAM ACCOMPLISHMENTS

The SSDR not only represents one of the first attempts at the design and fabrication of a large bubble memory but also it is probably the first attempt at applying the constraints of spaceborne design criteria to such a system. Because of this, a large amount of original basic conceptual design was required in the areas of system configuration, packaging and circuitry. Specific areas where critical design concepts have been developed and proven include:

Memory Cell - A multichip memory cell is a prerequisite for volume, power and weight critical bubble mass memory systems. The feasibility of a multichip cell design has been demonstrated both mechanically and electrically by the SSDR cell.

Cell Drive Circuitry - Direct cell drive circuitry including operator function drivers, coil drive and sense circuitry are obvious critical design areas. Volume and weight efficiency requires a matrixed approach to these functions to minimize parts count. Matrixed circuit configurations for operator functions and coil drive have been developed and proven feasible. A matrixed sense circuit design was developed and proven to be feasible in principle but subject to some problems in practice. This area is discussed further in Section 13.3.

System Organization - Two fundamental system concepts have been developed and proven that are basic to fully utilizing this technology. One concept is establishing the memory module as a basic building block for the memory system. The second concept is the use of a microprocessor based drive and control unit to act as an interface between user and memory module allowing a high degree of flexibility and configuration control.

13.3 PROBLEM AREAS

In assessing the performance of the SSDR, two problems may be classed as fundamental. The first problem is a limited operating temperature which is memory element related and the second is marginal sense performance resulting from both memory element characteristics and sense channel design.

Operating temperature limitations are basically a memory element material problem exhibited as a tendency for marginally high drive at low temperature and marginally low and nonlinear bias margins at high temperature. On a nominal basis, the memory element and circuit design appear to be just adequate to meet the intended temperature range. However, in the context of the statistical variation in parameters experienced over a large number of chips and production runs, insufficient nominal margin in excess of requirements exists to practically allow operating large numbers of memory elements over the intended -10 C to 60 C temperature range.

In the area of sensing, difficulty was encountered because of lower than anticipated detector sensitivity, dummy-active detector mismatch and adjacent bit noise. In addition to intrinsic detector performance problems, the sense channel design in terms of sense bus capacitance, sense bus isolation from system noise and sense amplifier selection added to sensing problems. Although the matrixing technique was proved feasible in principle, all of these factors rendered this particular sense circuit impractical without further improvements as recommended below.

13.4 RECOMMENDATIONS

The SSDR program has developed and proved a majority of the concepts required to establish the feasibility of bubble memory technology for spaceborne mass storage applications. Two areas requiring additional work prior to entering into design of flight hardware, are memory element operating temperature range and sensing. As a preface to discussing these two remaining problem areas, it is useful to discuss the intent and background of the SSDR program. This effort is basically a system design program and involved no memory element design effort. The element used in the SSDR was developed prior to the start of the program, thus, this memory element technology is about five years old. Recognizing the dynamic state of this technology, it is to be expected that present state of the art represents improved performance over that of the device used in the SSDR. Materials and propagation circuit elements developed during this five year period have resulted in operating temperature performance comfortably in excess of the SSDR temperature requirements with a lower drive field requirement. These improvements arise from the use of calcium germanium substituted bubble materials and gap tolerant propagation circuit elements. Utilization of a memory element based on the present technology should result in a straightforward and high confidence solution to achieving a wide operating temperature range.

A solution to the sense problem is not as straightforward as extending the temperature range. From a systems standpoint, three recommendations can be made. First, while the SSDR experience has demonstrated that multiplexing eight to sixteen cells is a viable approach, larger sense matrices will require detector impedances significantly lower than presently available technology can provide. Second, it would appear that neither core sense amplifiers nor plated wire sense amplifiers are suitable for currently available bubble memory detectors in a large system environment. Feasible approaches to bubble memory element sensing appear to be to implement a sense amplifier from available preamplifiers and comparators or develop a custom design integrated sense amp. A third system recommendation is to utilize a high degree of physical isolation between sense bus and other memory module electronics to minimize system injected sense noise.

At the memory element level, several approaches should be investigated to improve detector performance. Developing a detector approach which utilizes bits spaced two periods apart in the detector would significantly reduce adjacent bit noise in the detector. Such an approach would also allow back-to-back in-line active and dummy detectors as opposed to the guardrail detector used in the SSDR memory element. The close physical proximity of active and dummy detector should serve to minimize static and dynamic mismatch which was also a serious source of noise in the SSDR memory element. A final item to be considered in detector design modification is to raise the maximum allowable detector current, thereby producing a higher output voltage and an improved system signal to noise ratio.

At the system level, there are two areas which should be modified to provide the desired level of performance. One area involves the aspects of the DCU design which resulted in a limitation of data rate to 1Mbs/channel or 2Mbs composite data rate as compared to the design goals of 1.2Mbs channel and 2.4Mbs composite. As discussed in Section 11.0, this problem results from the length of the cycle counter overflow interrupt program during transition between cells. This particular software could be implemented in hardware without significant impact on parts count while providing a much more rapid execution of this function.

The second system area requiring attention is the power supply design. As discussed previously, this design was cost effective but inefficient in terms of weight, volume and power. An efficient power supply custom designed to the SSDR requirements will lower power consumption and reduce weight and volume.

In conclusion, it is recommended that the above suggestions be implemented and verified through the design and fabrication of a unified chip-cell-sense channel design. Successful completion of such a design modification in combination with the design and test experience gained on the SSDR program would serve as a high confidence base for design and fabrication of bubble memory flight hardware.

13.5 Current Effort

The DCU and power supply improvements recommended above can readily be accomplished by design changes using available electronic components. However, those improvements recommended in the memory module involve bubble technology and require some optimization. Current effort is in progress on this contract to incorporate these recommendations into a revised memory module design. Bubble chip redesign to improve the temperature range and tailor the chip detector for meeting the matrixing needs of large capacity systems has already been completed and a yield evaluation is in progress. In addition, the cell and memory module are currently being redesigned to reflect changes in the chip and provide improvements in the sense detection area. The redesigned chip, cell, and memory module will be discussed in a future report.

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15. Supplementary Notes

Langley Technical Monitors: R. L. Stermer, Jr., and Paul J. Hayes
Topical Report

16. Abstract

This report summarizes the results of a program to demonstrate the feasibility of Bubble Domain Memory Technology as a mass memory medium for spacecraft applications. The design, fabrication and test of a partially populated 10^8 Bit Data Recorder using 100 Kbit serial bubble memory chips is described. Design tradeoffs, design approach and performance are discussed.

This effort resulted in a 10^8 bit recorder with a volume of 858.6 IN^3 and a weight of 47.2 pounds. The recorder is plug reconfigurable having the capability of operating as one, two or four independent serial channel recorders or as a single sixteen bit byte parallel input recorder. Data rates up to 1.2 Mb/s in a serial mode and 2.4 Mb/s in a parallel mode may be supported.

Fabrication and test of the recorder has demonstrated the basic feasibility of Bubble Domain Memory technology for such applications. Test results indicate the need for improvement in memory element operating temperature range and detector performance. Current effort on this program is directed at improving these areas leading to flight hardware capability.

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